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Design of Single Electron Transistor (SET) and Implementation of Logic Gate using SET technology

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ABSTRACT
The Single Electron Transistor technology has attracted interest in VLSI designers for increasing the scalability and integration density. It is a step towards Ultra Large Scale Integration (ULSI), due to its potential of extremely low power consumption, nano scale dimensions and faster operating speed.

This paper presents a design & simulation of Single Electron tunneling transistor device. Also a design of simple logic gate inverter is also presented. This paper also discusses the approach for design of PLA, which is, layer of array composed of a SET summing inverter cell replicated for performing a programmable Boolean operations of its inputs. The design is based on hybrid SET/MOS logic which composed of complementary SET and CMOS logic. The SET/MOS hybrid circuit possesses the merits of SET circuit as well as MOS circuit.

The SET model is simulated using HSPICE. Logic design is using Multisim.

Keywords
PLA(Programmable logic array), SET(Single Electron Transistor), ULSI, SET/MOS Hybrid logic, SPICE.

1. INTRODUCTION
Feature size reduction and low power consumption has been an important contributing factor to the dramatic increase in processing power of logic and arithmetic circuits to increase the integration density of chip further. Therefore several emerging technologies are currently being investigated. One of them is Single Electron Transistor (SET) technology which offers a greater scaling potential than MOS as well as potential for ultra low power consumption.

This paper describes a circuit design for programmable logic array[2].Since by using PLA ,any Boolean logic can be implemented easily.

Herein we present a design using SET/MOS hybrid logic. The hybrid SET/MOS logic [2] has the advantages of both SET and MOS logic. Their advantages are as follows: 1) Compared with conventional circuits, the circuit's power dissipation is low 2) Compared with SET circuits, the circuit possess large load capability and large signal swing. And 3) they can be realized with modern silicon techniques

We are using SPICE macromodelling [5] to demonstrate the stable and correct operation of SET. The paper is organized as follows. Section II briefly describes SET background theory with its ideal characteristics. Section III specifies the design of custom component using SPICE macro model[6] of SET and inverter[4]design using SET/MOS[1] logic and discusses the issues regarding the proposed work to design PLA[2] and Section IV describes design challenges and future prospects using hybrid SET/MOS [3][5] logic and shows its simulation results.

2. SET BACKGROUND
The Single Electron Transistor technology [1] deals with the control and transport of single electron. The fundamental physical principles of single electronics are the tunneling effect and Coulomb blockade. SETs held great promise for future nano-electronic circuits due to their ultra small size, low power consumption and ability to perform fast and sensitive charge measurements.

3. BASICS
3.1 Single Electron tunneling effect
The basic structure of SET is shown in fig.1 below:

In single electron devices, electron travel to and from source to drain through a small conducting island as shown in above fig. The passage of single electron through island in these devices is possible by ensuring the following conditions. If the tunnel resistance is sufficiently high (i.e.>>h/e^2) approx.28.5kΩ.The quantum fluctuations becomes significant and the electron is localized on island.

The second condition is that the island is the total charging energy $E^2/2C_\Sigma$ (C_Σ=Cs+Cd+Cg)should be higher than thermal energy KT(K=Boltzmann's constant= Temperature in Kelvin).For ensuring second condition, island sizes of 1-5 nm which reduces tunnel junction capacitances to 10^{-19} af at room temperature is desired.

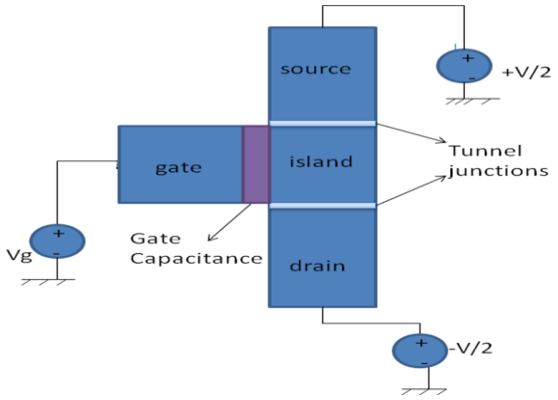

Fig.1 [1].Basic structure of SET

As the fig.2 shows the equivalent structure of SET showing tunneling resistances Rd and Rs, tunneling capacitances Cd and Cs.When compared with FET, the channel is replaced by tunneling junctions and a conducting island. The injection of an electron from source ro island under a positive applied bias Va>E/e i.e. $e/2C_{\Sigma}$.This potential barrier results in a coulomb blockade or the electron is travelling through island in a quantized way but not in a continuous way.

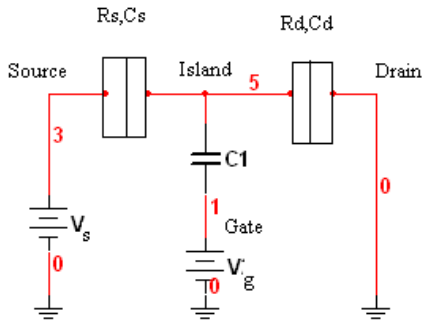

Fig.2. Equivalent structure of a SET

3.2 Characteristics of SET

The ideal V-I characteristics of SET simulated by Monte-Carlo method using well known single electron transistor simulator SIMON and spice simulation using Wu and Lin's model are shown in fig.3 .

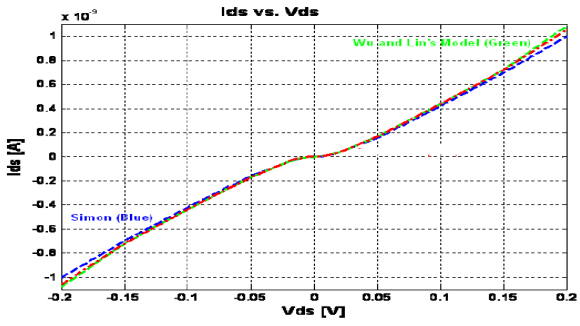

Fig.3 [6].Ideal o/p V-I characteristics of SET

In spite of the fact that the current flow in SET is quantized in nature, the characteristics above shows that that current linearly varies with applied bias voltage. It is because of the fact that ,for the given bias voltage the transition time required for tunneling of one electron through barrier is 10^{-15} sec.

3.3 SET/MOS Logic

3.3.1 SPICE macro-model

From a SPICE equivalent macro model of a SET by Wu and Lin is as shown in fig 4b. The resistances R1, R2 and R3 are the function of V_G and V_{DS} and are given as

$R1\ (V_G, VDS) = CR1+CR2\ [\cos\ (CF\times\pi\times V_G)+2^{|CVP-VDS|x}\ ]$ &

$R2\ (V_G, VDS) = R3(V_G, VDS) =CVP/\ (CI_2\text{-}CVP/R_1\ (V_G, VDS))$

Where, the parameter x is the function of temperature and the parameters CR1, CR2, CF and CV_P are given as below:

CR1 = 4Rj, CR2 = 1.33Rj, CF = 2Cg/e, CVP = 0.02

Here, Rj is the junction tunneling resistance and Cg is the gate capacitance.

A SPICE net list is created and a custom component called SET is designed in MULTISIM as shown in fig. 4a

The parameters [6] V1 (+Vp) and V2 (–Vp) specifies the range of the Vds where the current Ids is zero i.e. duration for which no current is flowing through the circuit is a region called "coulomb blockade" [5] region in the characteristics. Coulomb blockade is the property of SET transistor which allows the flow of a single electron through island.

A SPICE net list of above macro-model is created and simulated successfully in HSPICE and multisim. The simulation result is shown in fig.4c .Using this SPICE net list a custom component called SET is created in multisim. The symbol of this custom component SET is shown in fig.4a

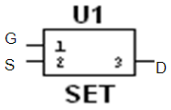

Fig.4a. SET as a custom component

3.3.2 INVERTER based on SET/MOS hybrid logic

An inverter based on SET/MOS hybrid logic is designed as shown in fig.5a and successfully simulated in MULTISIM.

Here, we have used SET with PSET i.e. SET which triggers with opposite polarity. The PSET is the SET itself in which when input is HIGH SET will conduct and PSET will be in coulomb blockade region. PSET forms a short circuit from VSS to output terminal and gives VSS as output. Reverse is true for LOW input.

The simulation result is shown in fig.5b

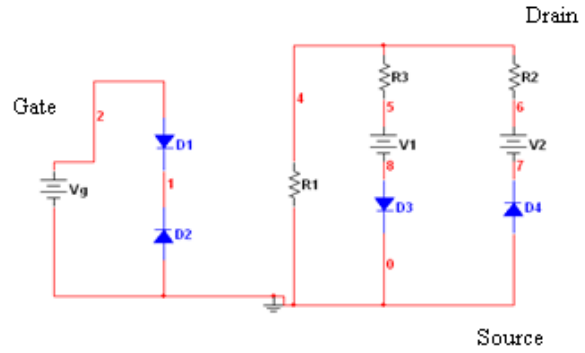

Fig.4b [2] .Proposed macro-model of Wu and Lin

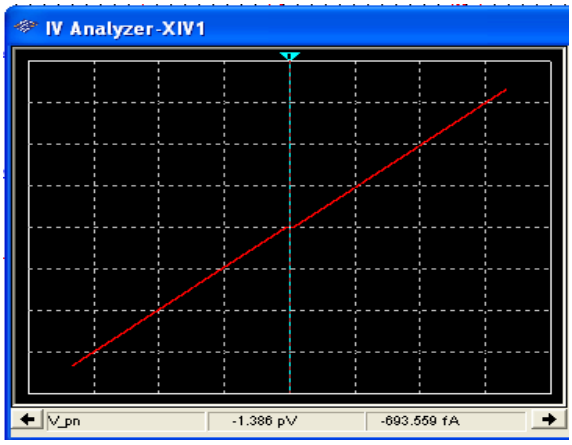

Fig.4c simulation result of SPICE SET model

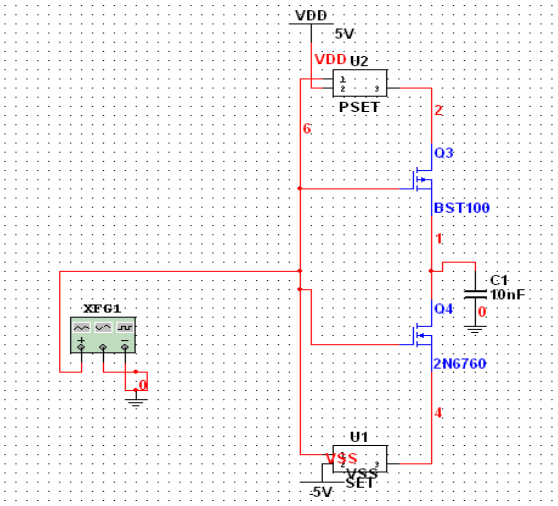

Fig.5a SET/MOS hybrid logic based inverter circuit arrangement

3.3.3 Proposed work

To design a summing inverter by using above designed inverter

To replicate above designed summing inverter or NAND logic so as to implement any boolean function

As shown in fig.6. The first layer generates the complement of the input signals using the inverter structures while the second layer consist of SET NAND replicas used to evaluate the product terms (BA')' and (B'C')'.The third

layer also combines the product terms to map the product terms into one NAND function F=((B.A').(B'C')')'

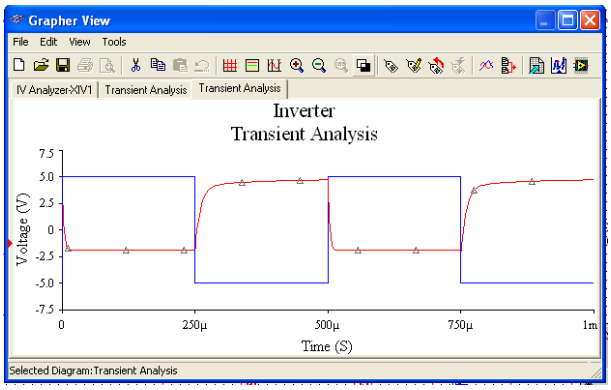

Fig.5b Simulation result of Inverter

4. CHALLENGES AND FUTURE PROSPECTS

The various challenges and future aspects regarding above approach are given as follows

a) The main disadvantage with SET devices is the difficulty at the present time to realize structures with sufficiently small capacitances such that they operate at room temperature

b) Moreover device to device variations for present structures are quite large which is an issue that has to be overcome by greatly improved process technology.

c) Another greater challenge is random background charge which denotes any charge close to any circuit to be disturbing but which is outside of the direct control making it virtually random

d) The signal gain of a SET transistor is a major concern since SET transistors have a very low gain

e) If a SET transistor is expected to replace MOS transistor, it must have a signal gain greater than one for a transistor feature size less than 10nm, which is not possible with such a small size

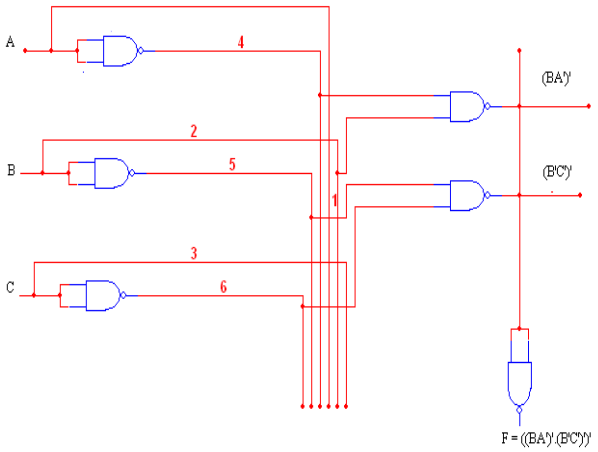

Fig. 6.PLA circuit layout in conventional logic gate

5. CONCLUSION

This paper investigated the use of SET devices in future nanoelectronic digital IC's.We discussed the design of SET/MOS hybrid inverter and a design concept to design a PLA style architecture using NAND/NOR gate array Logic using SET. We also have discussed the SPICE modeling for SET simulation. Finally, we concluded with Single Electron device challenges and future prospects regarding SET/MOS hybrid technology.

6. REFERENCES

[1] Konstantin K.Likharev"Single electron devices and their Applications", published in *Proc.IEEE*, Volume 87, pp-606- 632,April- 1999.

[2] Costa Gerousis and Arther Grepiotis, "Programmable Logic Arrays in Single Electron Transistor technology,"ICSES 2008 International conference on Signals and Electronic systems,Krakow,september-2008.

[3] Orin Cotofana,"Single electron tunneling based computation",27th international conference on microelectronics,16-19 May 2010.

[4] Kutsuhiko Degawa and Takafumi Aoki "A single electron transistor logic gate family and its application- part 1:basic components for binary,Multiple –Valued and Mixed mode logic"34th international Symposium on Multiple Valued Logic,2004 IEEE.

[5] Kutsuhiko Degawa and Takafumi Aoki "A single electron transistor logic gate family and its application- part 2:Design and Simulation of a 7-3 Parallel counter with linear summation and Multiple valued Latch Functions, 34th international Symposium on Multiple Valued Logic,2004 IEEE

[6] Mohammad Reza Karimian and Massoud Dousti,"A new SPICE Macro model for the simulation of Single Electron Circuita", Journal of the Korian Physical Society, Vol.56, No.4, April 2010, pp.1202~1207.