International Journal of Applied Information Systems (IJAIS) – ISSN : 2249-0868
Foundation of Computer Science FCS, New York, USA
2nd National Conference on Innovative Paradigms in Engineering & Technology (NCIPET 2013) – www.ijais.org

An Overview and Analysis of Low Power SRAM Design

R. A. Burange
Research Scholar,
B. D. College of Engineering
Sevagram, Wardha(MS), India

G. H. Agrawal, Ph.D
Professor, Electronics & Power Engineering,
KDK College of Engineering, Nagpur (MS), India.

ABSTRACT
Static Random Access memory (SRAM) is a matrix of static volatile memory cell. Different techniques used for power optimization and Challenges regarding reduction of static and dynamic powers are discussed. Power reduction of other supporting circuits like Sense amplifier is analyzed with respect to a standard design.

General Terms
Current Mode and Sense Amplifier, Low Voltage SRAM, Leakage power.

Keyword
static Random Access Memory(SRAM), Low Power, Bit Line, Charge Recycling, Low Swing.

1. INTRODUCTION
Memory is an important part of computer and microprocessor based system design. It is used to store data or information in terms of binary numbers. The data used in program and execution are stored in the memory. Therefore memory is required for temporary as well as permanent storage of data in digital system.

Memories are of two types RAM and ROM. ROM is a permanent memory. RAM is classified in two types SRAM and DRAM. Since memory is an array type of structure, so cost per bit of the memory decreases with the cell area. For smaller memory cells, we can achieve larger storage capacity in the given silicon area. Hence the technology with the smallest feature size available should be used for the memory design.

The aggressive technology scaling trend is driven by the requirement of large amount of inexpensive memories for most of the computing and networking applications [1]. CMOS is preferred due to its superior noise margin, scaling capability, mature process, worldwide availability, and low cost and low static power consumption [1, 2]. Static power consumption is worsening with the scaling of the technology due to significant reduction in threshold voltages. Hence it is more challenging to design the low-power SRAMs in the technologies 0.18um and below since the SRAM consumes significant static power due to sub threshold leakage [3].

1.1 Static Random Access Memory (SRAM)
An SRAM is matrix of static volatile memory cells, and it addresses decoding functions integrated on-chip to allow access to each cell for the read and write functions. The basic architecture of the SRAM contains one or more rectangular arrays of memory cells with control circuitry to decode addresses for few basic and special operations. Since memory densities are increased in mobile, hand-held and battery operated devices as well as data transfer rates, so these systems requires less power and high speed. Also memory currently makes up a large part of systems, nearly fifty percent, therefore reduction of power and delay in memories becomes an important issue. Memories are also responsible for almost half of the total CPU dissipation. This has been shown to be true in some of the more power efficient designs with on-chip memories. In cases like these it is necessary to determine the sources of power consumption and delay in memory blocks and cells so that they can be removed or reduced, allowing for better overall performance of the system. The power consumption can be reduced by adopting suitable techniques, such as circuit partitioning, increasing gate oxide thickness in non-critical paths, reducing Vth (dual Vth) etc. The circuit partitioning technique also improves the speed of our memory. The control block, the decoders and IO blocks are all in low Vth, whereas the memory cells, along with the sense amplifier are in high Vth[4].

2. MEMORY ARCHITECTURE
SRAM cell contains two cross-coupled inverters forming latch and the two access transistor connecting these invertors to the complimentary bitlines to communicate with outside the cell. The access transistor is the NMOS transistors. As long as the access-transistors are turned off, the cell keeps one of its two possible steady states. The schematic of the SRAM cell is shown Fig 1. In both read and write operation common word line (wl) signal controls the accessibility to the cell nodes q and qbar through two NMOS access transistors. Ideally all the cells are kept at low W/L ratio but a careful sizing is necessary to avoid accidentally writing word line is enabled for reading, the series combination of two NMOS transistor pulls down the BL' line to ground.

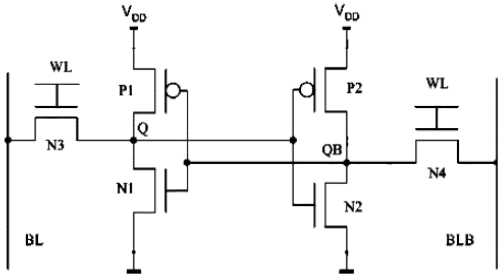

Figure 1: 6-T SRAM cell

3. Challenges and trends in Low voltage SRAM design.
*1.*Write Power: As per the analysis, it seems that the write power is substantially higher than the read power[5]. The graph depicts the same. During write operations, the charge-recycling operation is performed through BL pairs.

In BLs, the write power is much smaller than the read power. However, when the operation mode changes from read to write, the initial voltages of BL pairs are different. The reference voltage-generation circuit for the write pre-charge voltage levels has to be activated, whenever the mode changes from read to write. This results in power and delay overheads for the write startup.

2. Leakage Power: Power dissipation in CMOS circuits can be categorized into two main components - dynamic and static power dissipation. Dynamic dissipation occurs due to switching transient current (referred to as short-circuit current) and charging and discharging of load capacitances (referred to as capacitive switching current). Static dissipation is due to leakage currents drawn continuously from the power supply. There are various modes which contribute to leakage current, such as sub threshold leakage, reverse-biased PN junctions, drain-induced barrier lowering (DIBL), gate-induced drain leakage, punch-through currents, gate oxide tunneling, and hot carrier effects. However, the main contributor of leakage is the sub-threshold leakage current and is briefly discussed in this section. At sub-threshold level, it is seen that leakage power becomes comparable or almost equal to the dynamic power. The power estimation for SRAM with 256 rows and 256 columns build using 70nm technology is plotted in the following viewgraph [6]:

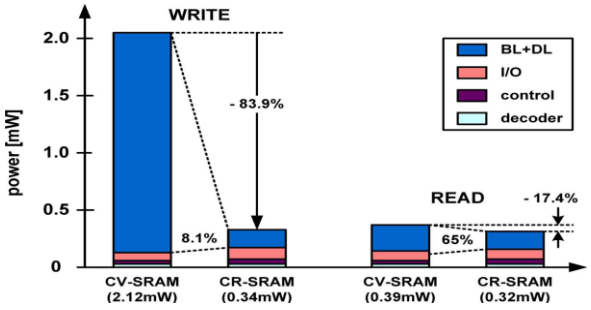

Figure 2: Write Power of SRAM

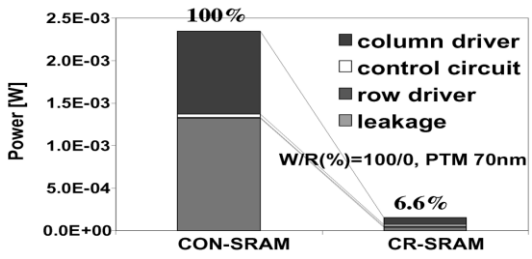

Figure 3: Leakage power and Dynamic Power

As visible above the leakage power is dominant factor in the complete power dissipation graph.

3. Sense amplifier power: There are a lot of sources of power consumption. The total delay is mainly determined by the significant capacitances attributed by the long-wire paths routed in close proximity (commonly known as and) [7]. These highly capacitive wires are also important factors that drastically increase the total power dissipation during the read and write operations. The current-mode SA, which has the ability to quickly amplify a small differential signal on the bit-lines (BLs) and data-lines (DLs) to the full CMOS logic level without requiring a large input voltage swing, is widely used as one of the most effective ways to reduce both sensing delay and power consumption of the SRAM.

The power dissipation caused by sense amplifier in [7] during read cycle of SRAM operation and propose a new current-mode sense amplifier to reduce the current during read operation as presented in below graph:

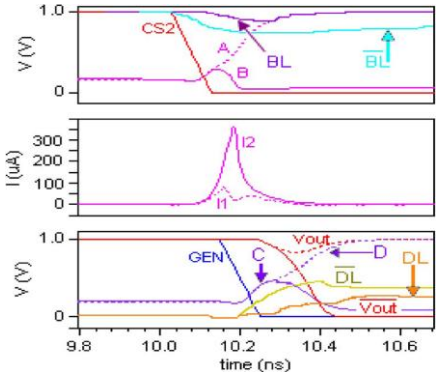

Figure 4: Current for read operation

4. Conventional 6-T SRAM cell limitations:

A conventional 6T SRAM cell consists of two inverters, inv1 and inv2, connected back-to-back and two nMOS pass transistors that are used to access the cell for read or write. For a stable write operation, setting one of the bit lines to "0" and the other to "1" is necessary. Careful transistors sizing is also required to ensure a stable read and write operations [1]. At a write operation, the probability of discharging one of the bit line pair equals "1" which means that the activity factor of switching the bit line pair equals "1." The bit lines' power consumption $P = \alpha_{BL}\, C_{BL}\, V^2\, F_{write}$ where $\alpha_{BL} = 1$.

The 7T cell reduces the activity factor to less than "0.5" and therefore, it exploits the fact that most of the bits in caches are "zeros" for both data and instruction memories [7,8] to reduce the write power consumption.

5. Increased capacitance: It has been noticed often that increased memory capacity increases the bit-line parasitic capacitance which in turn slows down voltage sensing and make bit-line voltage swings energy expensive. This result in slower and more energy hungry memories. The bit line has divided to reduce this capacitance resulting in less capacitance and also reducing the read time [9].

4. CONCLUSION

In this paper SRAM is discussed, it seems that there is a lot of scope of improving the performance and reduction of power of SRAM circuits. Combination of different techniques can result in optimization of low power SRAM that shall result in better power consumption than any of the discretely deployed technique.

For instance the leakage reduction techniques mentioned and can be combined with which increase in speed/performance of SRAM by reducing the bit line capacitance. A detailed analysis of SRAM with multiple optimization techniques can then presented for the user to decide how many techniques shall be used to achieve a optimized minimal power

dissipation and still keeping the performance above threshold value.

5. ACKNOWLEDGMENTS

The author would like to thank the anonymous reviewers whose feedback helped improve the quality of this paper.

REFERENCES

[1]Andrei Pavlov and Manoj Sachdev, "CMOS SRAM Circuit Design and Parametric Test in Nano-Scale Technologies", 2008 Springer Science Business Media B.V.ISBN 978-1-4020-8362-4 e-ISBN 978-1-4020-8363-1.

[2]Jawar Singh, Jimson Mathew, Saraju P. Mohanthy and Dhiraj K. Pradhan, "Single Ended Static Random Memory for Low-Vdd, High-Speed Embedded Systems",22nd International Conference on VLSI Design 2009.

[3]Bharadwaj S. Amrutur and Mark A. Horowitz, "Speed and Power Scaling of SRAM's", IEEE Transactions on Solid-State Circuits, vol. 35,pp. 175-185, no. 2, February 2000.

[4]Sreerama Reddy G M and P Chandrasekhara Reddy, "Design and Implementation of 8K-bits Low Power SRAM in 180nm Technology", Proceedings of the International Multi Conference of Engineers and Compute Scientists 2009 Vol. II IMECS 2009, March - 20, 2009, Hong Kong.

[5]Byung-Do Yang, "A Low-Power SRAM Using Bit-Line Charge-Recycling for Read and Write Operations", IEEE journal of solid-state circuits, vol. 45, no. 10, October 2010.

[6]Keejong Kim, Hamid Mahmoodi, Member, IEEE, and Kaushik Roy, Fellow, IEEE.,"A Low-Power SRAM Using Bit-Line Charge-Recycling", IEEE journal of solid-state circuits, vol. 43, no. 2, February 2008.

[7]Anh-Tuan Do, Zhi-Hui Kong, Kiat-Seng Yeo, and Jeremy Yung Shern Low, " Design and Sensitivity Analysis of a New Current-Mode Sense Amplifier for Low-Power SRAM". IEEE Transactions on Very Large Scale Integration (VLSI) systems, vol. 19, no. 2, February 2011

[8]Ramy E. Aly and Magdy A. Bayoumi, Fellow, IEEE,"Low-Power Cache Design Using 7T SRAM Cell", IEEE Transactions on circuits and systems—II: express briefs, vol. 54, no. 4, April 2007.

[9]Kavita Khare, Nilay Khare, Vijendra Kumar Kulhade, Pallavi Deshpande, "VLSI Design And Analysis Of Low Power 6T SRAM Cell Using Cadence Tool", IESE 2008 Proc.2008, lohor Bahru, Malaysia.

[10]"A Low-Power SRAM Using Bit-Line Charge-Recycling for Read and Write Operations" by Byung-Do Yang, IEEE Journal of solid-state circuits, vol. 45, No. 10,pp. 2173 - 2183, October 2010.

[11]"Design of a High Performance and Low Power 1Kb 6T SRAM using Bank Partitioning Method" by Kumkum Verma, Sanjay Kumar Jaiswal and Mohammad Ayoub Khan, 2011 International Conference on Multimedia, Signal Processing and Communication Technologies, pp. 56 -59.

[12]"A Low-Power Embedded SRAM for Wireless Applications" by Stefan Cosemans, Student Member, IEEE, Wim Dehaene, Senior Member, IEEE, and Francky Catthoor, Fellow, IEEE, Journal of solid-state circuits, vol. 42, No. 7, pp. 1607 -1617 , July 2007