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Machine Learning Adaptation in Post Silicon Server Validation

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ABSTRACT

As the complexity of modern server processors increases so the validation challenges. Current design validation methods cover less, resulting in bug escape and more regress post-silicon validation. The biggest problem is manual debugging of several failures by large number of test cases. By using machine learning in server validation, validation efforts and resource requirement will reduce. Validation of future generation server will be done through the learning set generated from the previous generation device, which is a set of test cases being passed.

General Terms

Algorithm, Machine learning, Validation.

Keywords

Debugging, Learning set, Machine learning, Post-silicon, Server, System under test (SUT), Validation.

1. INTRODUCTION

Machine learning is a inter discipline concept which models a particular problem using the given input and output data sets instead of using the underlying system information like actual system equations, responses etc [1]. In many real world problems knowing the underlying system dynamics and building the ideal system model is not trivial, in such scenarios usage of machine learning techniques eases the modeling task. Many practical problems tolerates the imprecision, uncertainty and approximations so these problems does not need the conventional hard computing techniques [2].

Many of the machine learning algorithms are inspired directly from the nature. Artificial neural networks uses the brains massive parallelism, Fuzzy logic uses the human vague thinking, Genetic algorithms adopted the survival of fittest concept, Simulated Annealing uses the slow cooling process in metallurgy etc. So machine learning algorithms also known as soft computing methods [3].

Machine learning algorithms are classified into several forms based on how the algorithm treated the inputs. These are supervised learning, unsupervised learning, etc. Nowadays machine learning are used in many areas like OCR, medical diagnosis, stock market analysis, data mining, computer vision, search engines[4]. The system validation field has been slower to adopt modern machine learning techniques to the degree seen in other fields.

2. INTRODUCTION TO POST-SILICON VALIDATION

The complexity of modern computers and servers has increased to a very high level. The recent cutting edge technology processors and servers contain the billions of transistors, and they should be compatible with all operating systems, platform components, all input/output peripherals and all software applications. To get a better performance, reliability, quality and compatibility in such a complex environment, Intel performs system validation. Post silicon System validation mainly needs because of two reasons. Complexity of processor architecture & design grows exponentially, Pre-silicon validation is not enough to get comprehensive coverage.

Post silicon validation is mainly used to find and fix bugs in ranging from small chip to a big systems. This validation is mainly done after manufacture of chips and systems, because it is impossible to detect and fix bugs before manufacture due to high complexity of platforms and systems. Post silicon validation mainly involves running of actual applications on systems after manufacture, for a long time over a specified operating conditions to meet the industry accepted specifications specified by manufacturer. In future post-silicon validation is very difficult because existing methodologies cannot cope with high complexity of future systems [5].

Post silicon validation mainly involves four steps: 1.Large number of test suites ranging from small instructions to end user applications like verification of device drivers, operating systems, hardware and software specifications like advanced configuration and power interface specifications, are applied to a system under test(SUT). 2. After running for a long time to create system stress and for functional validation, have to verify any failure occur or not. 3. If any failure occurs, problem is need to be identified and localized to a small region of the system. 4. After that identifying the root cause of the problem and fixing the problem is the final step of post silicon validation.

The method used in post silicon validation is pseudo random multi master concurrency. A master is nothing but it can have the capability to generate a system traffic. Masters can be a CPU devices, any input or output devices. These devices are used to generate traffic by moving data from one device registers to another device registers. By this way system stress can be created with the use of more number of masters. In order to validate a computer system, need to verify large number of bus transactions and logic states and this is very difficult to validate. In order to simplify validation, tests are randomly generated. Generation of tests is not truly random, but it is a pseudo random, because whenever a failure occurs it need to reproduce it. This is very useful in such a debug situation. By applying large number of tests system stress is maximized. By maximizing system stress, failures or bugs will be determined. According to system failure, identifying the root cause of the problem and fixing that problem by patching and circuit editing etc. with the design team is the final step of validation

3. SERVER VALIDATION CHALLENGES

As technology goes on increasing the platforms or devices developed are getting more complex. For validating such a more complex devices also getting difficult to manage. For those devices there are many number of tests have to apply for validation. Checking each test results manually is also difficult. Managing such a large number of test cases for validating each next generation devices is very difficult. Introducing machine learning in the field of system validation to validate future generation servers it will be useful.

A learning set from a known validated device is a set of test cases which are passed. This learning set is useful for validating next generation devices with a set of new test cases. While validating new devices, learning set is updated by using the algorithm described below in Figure 3. This algorithm is developed based on the Venn diagram described in Figure 1. So each time learning set which is developed from a known device, is used to validate next generation devices. By this way validation of systems is done.

4. VALIDATION METHODOLOGY OF SERVERS

Already mentioned in last section that for validation of future generation servers managing of large number of test cases is very difficult. Venn diagram shown in Figure 1 is used to automate the validation. Validation of system is done in two phases.

4.1 Learning set preparation for a known valid server

In the Figure 1, Universal test cases are inclusive of all the tests independent of system and result. So for validation of future generation of servers, preparation of learning set is required. Learning set is a set of test cases passed for a valid known device (A) i.e. means the device was already validated, otherwise it is a set of genuine test cases passed. The block diagram for learning set preparation is shown in Figure 2.

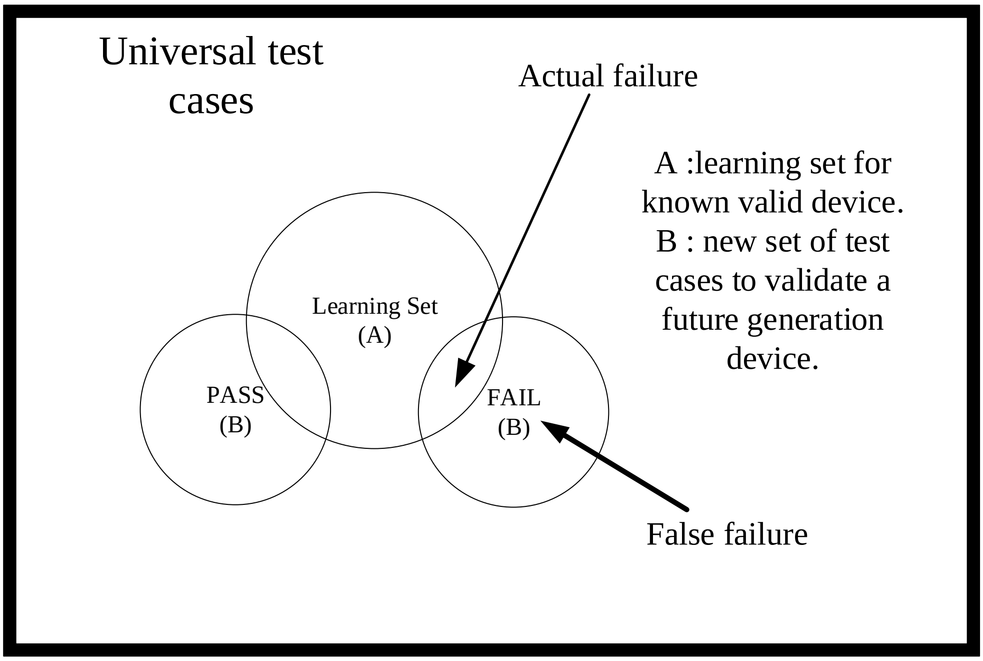
Universal test cases
Actual failure
A :learning set for known valid device.
B : new set of test cases to validate a future generation device.
Learning Set (A)
PASS (B)
FAIL (B)
False failure

Fig 1: Test cases Organization

Steps for preparing the learning set:

- Select the known valid server or SUT(system under test)
- Apply the test then obtain the result & log the result.
- Verify whether it is passed or not.
- Prepare the learning set depends on the result.
- Learning set is a dictionary containing pairs of tests and results.
- If test is passed add it to the learning set.
- If it fails, the test is not a valid test and apply another test.
- Repeat the above steps until all the tests are over.

The final learning set obtained is used to validate the future devices.

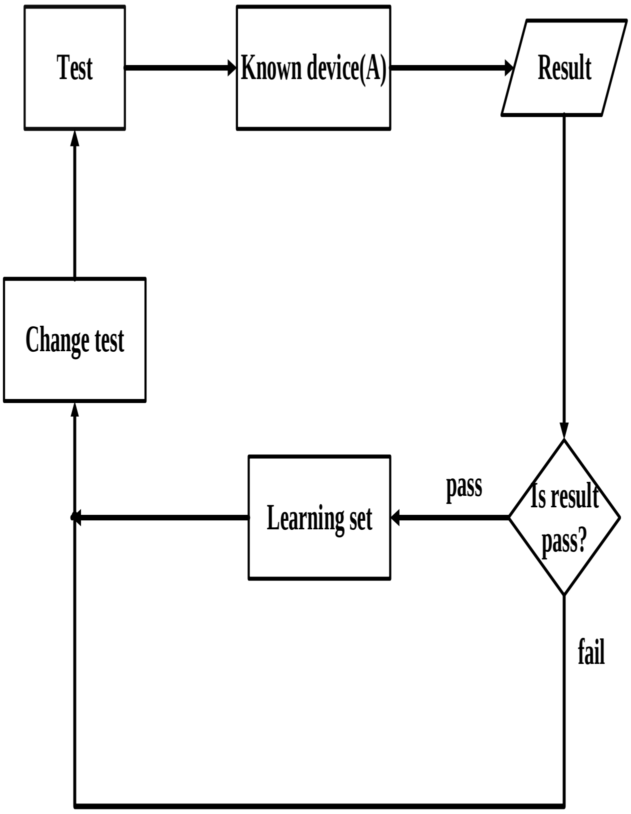

Fig 2: Learning set preparation for a known valid device (A)

4.2. Proposed Algorithm for validating SUT and updating the learning set

Proposed algorithm is shown in Figure 3. Steps for validation of server (SUT):

- In the algorithm shown in Figure 3, each time a new test case applied to system under test (SUT).
- Result obtained is verified, whether it is pass or fail.
- If it passes, then update it on the learning set, else check whether the test case is in the learning set or not.
- If it is present in the learning set then it is called “actual failure”. If it is not present in the learning set then verify whether the test case is a new feature or not.
- If the test case is new feature then update it on the learning set, else the failure is called as “false failure”.
- Actual failure logs are useful in debugging and to fix the failures.
- For the actual failures, identify the root cause and work around it.
- Repeat this process until all the test cases are finished.

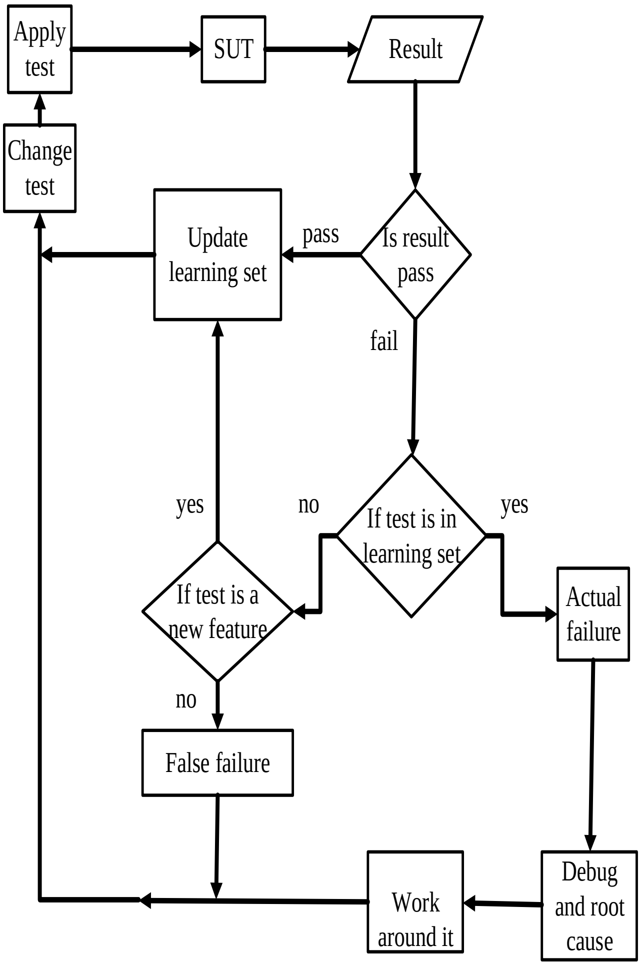

Fig 3: Algorithm for validating SUT and for updating learning set

By using the above algorithm validation of future generation servers is performed. Validation is done using the above two phases. In the first phase mainly deals with computing learning set which is obtained by validating known valid device. By using this learning set in the second phase, validation of next generation server (SUT) is done. While validating this server updating learning set will be useful for further generation server.

5. CONCLUSION

Introduction of machine learning in the server validation simplifies validation methodology and reduces man power. Validation of new server processors is done through two phases. In the first phase mainly deals with computing learning set which is obtained by applying test cases to known valid device, which is a set of test cases being passed. The next generation server (SUT) is validated by using above computed learning set. While validating this server learning set is updated, which is useful for validating future generation servers.

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