International Journal of Applied Information Systems (IJAIS) – ISSN : 2249-0868
Foundation of Computer Science FCS, New York, USA
Volume 6 – No. 3, September 2013 – www.ijais.org

Investigation of the Electronic -Properties of Al-CdTe-Au Schottky Diode

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ABSTRACT
In order to interpret the effect of semiconductor thickness and annealing temperature on the electrical characteristics of Al/n-CdTe/Au Schottky barrier diodes (SBDs), the forward and reverse bias current density-voltage (J-V) characteristics of these SBDs have been investigated in dark. Both of the values forward and reverse currents have decrease with increasing annealing temperature as well as the increase of thickness. The ideality factor (η), saturation current density (J_s) and the barrier height (Φ_B) were calculated using J-V plots. Also series resistance (R_s), shunt resistance (R_{sh}) has been calculated by R-V plots. The measurements showed that these parameters are affected by annealing temperature and the change in the thickness.

Keywords
Au/n-CdTe, I-V characteristics, series resistances, shunt resistances.

1. INTRODUCTION
Cadmium telluride (CdTe) is an important group II–VI semiconductor with a direct band gap and close to the visible region; it has a high absorption coefficient which is required for good theoretical conversion efficiency [1]. Extensive research was done in the last two decades on CdTe thin films, mainly due to its potential applications, in optoelectronics. The Schottky junction is one of the fundamental structures in electronics and finds application in electronic devices like low-voltage, high-current rectifiers [2]. Metal/CdTe interfaces play an important role in opto-electronic devices and have been studied by different research groups. M. G. Mahesha et al. [3] have studied junction behavior of evaporated Al/CdTe They have found that at lower bias voltages, current conduction is by thermionic emission where as at higher voltages, current is controlled by space charge limited conduction. Also they have observed that the junction capacitance and resistance of the Schottky junction decrease almost exponentially with frequency. H. Kanbur et al. [4] have studied the forward and reverse of Au/n-CdTe Schottky barrier diode are performed in the dark and under illumination at room temperature. They have found that the main electrical parameters such as I_s, η, Φ_B, R_s and R_{sh} obtained from I-V data were found strongly dependent on the illumination levels and while the values of I_s and n increase, Φ_B, R_s and R_{sh} decrease with the increasing density of illumination level. In the present study the forward and reverse bias J-V measurements of AL/n-CdTe/Au Schottky barrier diode are performed in the dark at 323k and after annealing temperatures with different 5thickness.

2. EXPERIMENTAL
In this work we have prepared Al/CdTe/Au structures by using CdTe (99.99% pure) (n-type) with Electron affinity (4.4eV) as a semiconductor substrate and we choose the (Al) with work function (4.13 eV) as ohmic contact and Au with work function (5.1 eV) as Schottky contact.
First we cleaned glass substrates of dimension (25.4x76.2mm thickness) by using soap-free detergent and followed by multiple rinsing in boiling water then rinsing in distilled water to remove traces of detergent, and then the substrates were cleaned in an ultrasonic cleaner for 15 min with ethanol. The last step of clean was drying the substrates.
The layers of aluminum were deposited by thermal vacuum evaporation using Balzer's coating unit model (BL 510) at pressure less than 10^{-5} mbar on glass substrate with a thickness 200nm. The evaporation process was performed in vacuum enclosure which provided with the necessary arrangements like evaporation source (Mo boat), movable substrate holder and radiant heater, were fixed inside the chamber. CdTe film was also grown by thermal evaporation method (Edward 306 Å) at 323k with thickness of the order 500 nm and 600nm done by using vacuum system model. Structural study was determined by X-ray diffraction analysis (Model XRD-6000, Shimadzu, Japan) using Cu-Kα (λ=1.54 Å). The Schottky barriers were prepared by vacuum evaporation of gold on front side of the CdTe with a thickness 40 nm. after that we annealed the samples under (375K, 437 K) and (10^{-5} Torr) pressure in vacuum for (30 min).

3. RESULTS AND DISCUSSION
X-Ray diffractogram of the CdTe thin film grown at 323k is shown in Figure 1. It reveals that film is in cubic structure and a strong preferred <111> orientation of micro crystallites. The

grain size of the crystallites (G) has been estimated using the following relation [5]:

$$G = \frac{0.94\lambda}{\beta \cos\theta} \quad \ldots (1)$$

where λ is the wavelength of X-Ray used, θ is the Bragg's angle and β is the FWHM of the peak. It has been observed that the grain size of the film increases from 12.8 to 20.1nm with thickness increased.

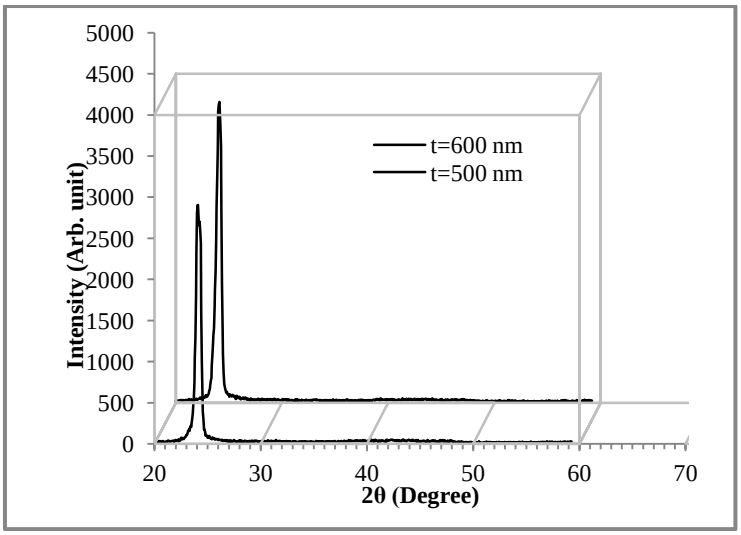
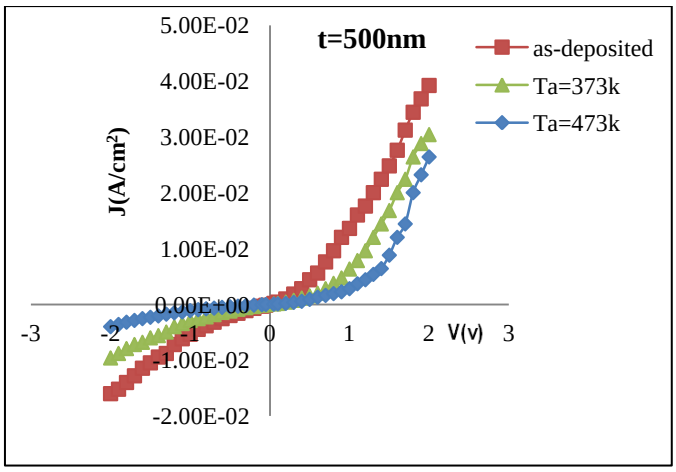


Fig 1: XRD CdTe Thin film deposited at 323k

To get Schottky diode between a metal and n-semiconductor, the work function of metal Φ_m must be larger than that of semiconductor Φ_s [6, 7]. Thermally evaporated Au film on CdTe thin film has been found to produce schottky contact.

The J-V characteristic of the Al/CdTe/Au Schottky junction at forward and reverse bias voltage as deposited and for different annealing with different thickness is shown in the Figure 2.



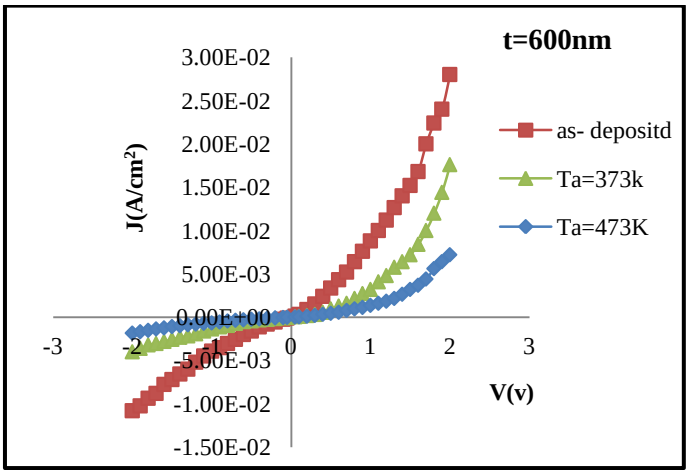


Fig 2: J-V characteristic for Al/n-CdTe/Au at forward and reverse bias voltage at different thickness and annealing temperatures.

From figures (2), it can be seen that the curve exhibit a highly non- linear feature. The non-linearity of J-V characteristic indicates that the prevalent conduction mechanism is non-ohmic in nature. For comparison two figures above show that at a fixed voltage, the magnitude of current density (J) decreases with increasing semiconductor thickness and increasing in annealing temperature which is attributed to increase in the depletion region width, and to improve in crystal structure by increase and decrease in the crystalline grain size [8].

The LnJ-V curves of Al/n-CdTe/Au schottky barrier diodes (SBD_S) are shown in figure (3). In general, according to the thermionic emission model, the relationship between the applied-bias voltage and the current through a barrier between metal and semiconductor junction can be analyzed by the following equation [4, 7]:

$$J = J_s \exp\left(\frac{qV}{\eta kT}\right)\left[1 - \exp\left(\frac{-qV}{kT}\right)\right] \quad \ldots (2)$$

Where V is the applied bias voltage on the SBD, η is an ideality factor and J_s is the saturation current density derived from the straight-line intercept of LnJ at zero bias is given by:

$$J_s = A^*T^2 \exp\left[\frac{-q\varphi_B}{kT^2}\right] \quad \ldots (3)$$

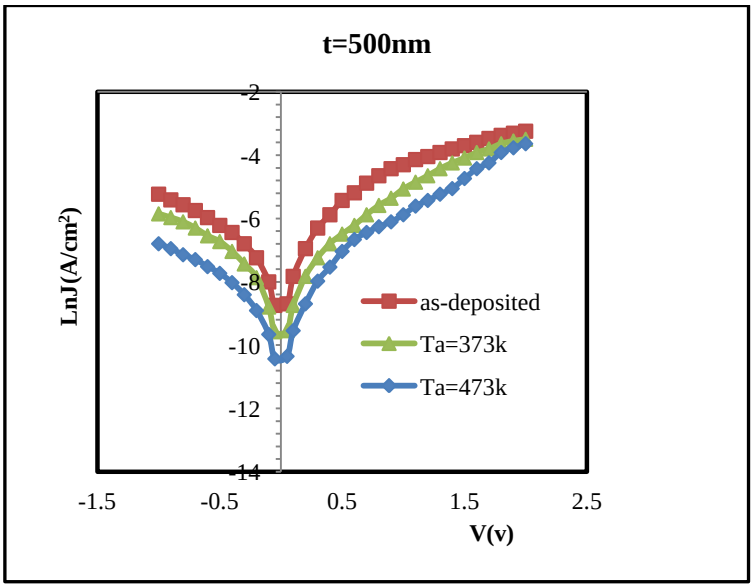
where Φ_B is the zero-bias barrier height, A is the rectifier contact area, A^* is the effective Richardson constant and equals to 12 A cm^{-2} K^{-2} for n-type CdTe, T is the absolute temperature in Kelvin and k is the Boltzmann constant. The ideality factor is calculated from the slope of the linear region of the forward bias LnJ-V plot and can be written from Eq. (2) as:

$$\eta = \frac{q}{kT}\left(\frac{dV}{dLnJ}\right) \quad \ldots (4)$$

Where dLnJ/dV is the slope of linear region of LnJ vs. V plots.

The value of Φ_B is calculated from the extrapolated J_s at zero according to following equation as:

$$\Phi_B = \frac{kT}{q}\ln\left(\frac{A^*T^2}{J_s}\right) \quad \ldots (5)$$



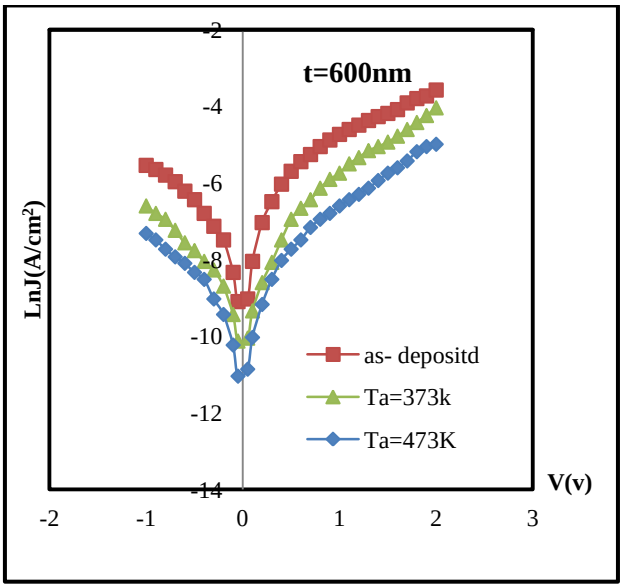


Fig. 3: Ln J-V characteristic for Al/n-CdTe/Au at forward and reverse bias voltage at different thickness and annealing temperatures.

The determined values of the, ideality factor, saturation current density, barrier height, series resistance, shunt resistance, at different thickness and annealing temperatures are shown in Table 1.

Table 1. The values of various parameters for AL/n-CdTe/Au SBD_S obtained from I-V data at different semiconductor thickness and annealing temperatures.

t (nm)	T(k)	J_S*10^{-5}(A)	η	Φ_B	R_s (kΩ)	R_{sh} (kΩ)
500	as- deposited	50	3.8	0.537	4	25
	373	30	3.4	0.55	5	58
	473	20	3.3	0.56	5.5	138
600	as- deposited	40	3.6	0.54	6	35
	373	15	3.33	0.567	10	100
	473	8	3.2	0.583	20	250

From figures (3) and table (1) shows the η of Al/n- CdTe /Au SBD is considerably larger than unity. The high value of ideality factor indicates that the junctions were non-ideal and most of the carriers (of electrons and holes) recombine at the junction (depletion) region. On the other hand, there can be many reasons to get junction ideality factor greater than unity; Henish H. K. [8] attributed this to the presence of an interfacial layer, image force lowering of barrier height, Sarmah and Rahman [3] attributed to the presence of an interfacial layer and tunneling effect. Bayhan and Erecelebi [9] attributed the increase of (η) to the series resistance effects which are associated with the neutral region of the semiconductor (between depletion layer and ohmic contact). Surface defects produce electronic energy levels in band gabs of CdTe semiconductor. These levels can pin the Fermi energy at metal-semiconductor interface and cause Schottky-barrier formation.. Also we found the value of η and J_s it decrease with increasing annealing temperature and thickness.

From table (1) that there is an increasing in the barrier height with the increasing of the annealing temperature and increase semiconductor thickness. The probable reason for this increase is that the metals disperse intimately during annealing and ensure a chemical reaction at the interface between the metal and the CdTe [10], and we can also note that the values of Φ_B deviate from the expected value and the cause for this in their study is non-stoichiometry on the surface. Only for stoichiometric surfaces, the barrier height depends on the work function of the metal, whereas this is not so for non-stoichiometric surfaces [3, 11]. Also the thin oxide layer formed between metal and semiconductor on exposure to atmosphere has been reported to influence the barrier height. This layer may be considered to be an insulator, even though it may be so thin that it does not possess the band structure which is the characteristic of thick oxide. Because of the potential drop in the oxide layer, the zero bias barrier height will be lower than it would be in an ideal diode, provided there is no charge contained in the layer. Also when a bias is applied, part of the bias voltage is dropped across the insulating layer so that the barrier height Φ_{B_0} is a function of the bias voltage [11].

Another important factors in table (1) and figure (4) are the presence of a series resistance R_S and shunt resistance R_{sh}, were obtained from the I-V data both in different annealing and different thickness using Ohm Law (V/I) [3]. The value of R_s and R_{sh} increases with increasing the thickness as well as increases with increasing the annealing temperature in the

voltage range measured and these changes are effective especially more significant at low forward bias and high reverse bias regions.

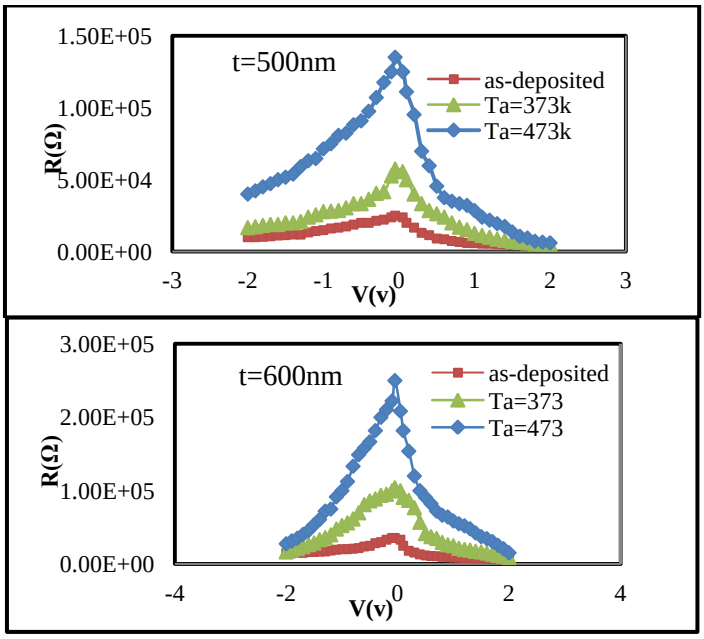


Fig. 4: R-V characteristic for Al/n-CdTe/Au at forward and reverse bias voltage at different thickness and annealing temperatures.

4. Conclusions

Cadmium telluride films deposited at substrate temperature of 323k are cubic in structure with strong preferred <111> orientation of micro-crystallites. The main electrical parameters of Al/n-CdTe /Au Schottky diode such as J_s, η, Φ_B, R_s and R_{sh} obtained from I-V data performed in dark were found strongly dependent on the annealing temperature and on semiconductor thickness and while the values of j_s and η decrease, Φ_B, R_s and R_{sh} increase with increasing the annealing temperature and semiconductor thickness.

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