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FFT Spectrum Analyzer using Goertzel Filter

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ABSTRACT
In this paper, the implementation of DSP algorithms on FPGA devices are taken into consideration and the FFT spectral analysis as a real time application was tested in MATLAB System Generator. It integrates two separate fields Digital Signal Processing (DSP) and Very Large Scale Integration (VLSI). The structure and chronological procedure followed focuses on the sophisticated DSP design and implementation of a Fast Fourier Transform (FFT) spectrum analyzer. The entire system was implemented in MATLAB Simulink Xilinx System generator (SG) toolbox. After simulation, the verilog coding was extracted and implemented on FPGA Virtex II device. As a part of betterment, FIR filter of the analyzer was replaced with Goertzel filter in order to improve the area efficiency of the FPGA device. It provides better frequency resolution and helps in extracting the amplitude component of the signal, thus aiding in improved spectral analysis.

Keywords
Coordinate Rotation digital computer (CORDIC), Digital Signal Processing (DSP), Direct Digital Synthesizer, FIR filter, Field Programmable Gate Array (FPGA) devices, Goertzel Filter, Mixer, windowing

1. INTRODUCTION
A spectrum analyzer is a device that measures the power spectral density of a signal, example power harmonics or one of numerous narrowly associated signal parameters. It processes an input signal to split and measure the individual spectral components of the signal, and order them according to their frequency. It scrutinizes the spectral composition of electrical, acoustic or optical waveform. The spectral analyzer measures the amplitude components of a complex waveform throughout its frequency range of the waveform. It is used in most of the signal processing system for measuring the distribution of signal energy in frequency.

Spectrum analyzer fall in two categories sweep type analyzer and Fast Fourier transform based spectral analyzer. In sweep type analyzer a local oscillator continuously executes the frequency sweep operation. A frequency spectrum component included in the signal to be measured is converted, by the frequency sweep operation, into an intermediate frequency signal consisting of a constant frequency component, and the power of the intermediate frequency signal is determined. It is based on the use of mixer and variable frequency oscillator. The input signal to be analyzed is mixed with the output local oscillator to produce the primary intermediate frequency signal. These analyzers implements cascaded band pass filters in combination with mixer to measure the signal amplitude at a given frequency. Thus a plot can be obtained between magnitude and frequency. Time required for one frequency analysis must be longer when the frequency resolution is made higher. This is the main disadvantage of this type of spectrum analyzer. Moreover these are non-real time instruments which can only be used to study a signal containing the frequency component within the sweep window and calculate the power of that frequency.

On the other hand a Fast Fourier transform spectrum analyzer analyzes the response characteristic of an electrical device or a mechanical device when supplied with a test signal. These analyzers are real-time analyzers that can overcome the limitations of a sweep frequency analyzer by simultaneously monitoring the entire band of the signal, by means of cascaded finite impulse response or infinite impulse response filters. Such real time spectral analyzer employs digital signal processing techniques, which sample and quantize the signal in time domain. Two environments are being used, Xilinx system generator in MATLAB Simulink for modeling the system and a hardware description language for performing the hardware implementation on a field programmable gate array devices. In this paper modeling of the Fast Fourier Transform spectrum analyzer is performed in Xilinx System Generator and implemented on field programmable gate array device (FPGAs).

FPGAs have increasingly become popularas it indicates a faster growth of its transistor density, compactness than general purpose processors. These electrical programmable elements can be used as basic electronic devices to implement low level operations. They also have the potential to implement much more complex systems dedicated to perform excessive time consuming computation processes. Therefore, a very high logic density and in system programmability offer designers low cost and powerful tool for VLSI implementations of circuits with short lead times, which turn FPGAs into a very useful design platform for rapid prototyping. A Virtex II FPGA device is used.

2. BRIEF DESCRIPTION
The Fast Fourier Transform spectrum analyzer consists of two 14 bit analog to digital converter (ADC). One of these ADC is used for the input signal to be analyzed and while the other for input signal phase increment through Direct Digital Synthesizer (DDS).

DDS generates highly accurate and harmonically pure digital representation of signals by accumulating phase changes at much higher frequency. The sampling theory requires the generated frequency to be less than half of the clock frequency (Nyquist rate). It is based on coordinate rotation digital computer (CORDIC) algorithm which is used for phase to amplitude conversion. As the signal gets generated in digital domain, it can be manipulated with excellent accuracy thus providing accurate control of frequency and phase.

The mixer stage is followed by cascaded band-pass digital finite impulse response (FIR) filter which are designed by impulse response truncation technique. It is designed to have a linear phase response which means signal in the pass band suffers no dispersion. The FIR filter is replaced by Goertzel filter as a part of betterment of analyzer design. It thus helped in better frequency resolution and faster detection time.

External control of windows function through random access memory cannot be performed once windowing technique is used for filter designing method. Designing of FIR filters involve various errors and noise. Primarily the noise arises due to A/D conversion which causes quantization error that reduces the SNR output. It can be avoided by increasing the number of bits in the ADC stage. Coefficients quantization is another prime source of noise which changes the parameters of transfer function and consequently the corresponding frequency response of the filters. Applying floating point arithmetic bypasses such noise occurrences. The filter is designed using FDATool present in signal processing block set.

The subsequent stages describe the process of implementing dual port or single port Random Access Memory (RAM) and Read Only Memory (ROM) blocks. Multiplexers to enlarge lookup tables (LUTs) based on combinatorial logic or memory are taken into consideration. FFT is the core block of the analyzer which is based on butterfly structure operation. Decimation in time and decimation in frequency are the two approaches to implement Radix -2, Radix – 4, Radix-8 or Radix butterflies processors which can be employed based on hardware resource utilization. CORDIC, an iterative algorithm is used for rectangular to polar conversion of the transformed values and for the computation of the natural algorithm to represent the spectrum in logarithmic scale.

3. WORKING

Analogue voltage varying from -1V to +1V is passedthrough 14 bit analog to digital converter as input signal. The signal is digitally processed in digital mixer where frequency shifting of the input signal spectrum is done using direct digital synthesizer (DDS v5). The spectrum resolution is adjusted by a three cascaded half band finite impulse response filters. The Fast Fourier Transform (FFT) core computes the FFT using radix algorithm and returns the complex transformed values. The modulus of the signal calculated using CORDIC algorithm is measured on logarithm scale. Finally, the analog signal is obtained using digital to analog converter and displayed in an oscilloscope. Gain of the CORDIC block used to compute the modulus and scaling in the FFT are compensated by adding a constant to the output. Since the system generator (SG) library does not include a log 10 module, the operation is performed by using a natural logarithm and adding supplementary multiplier by constant. The output is represented in equation 1 [4]:

$$\log_{10}(out * C_{FFT} * C_{CORIDC}) = \log_{10} out * 1024 * 0.6072$$

$$= \frac{\ln(out) + \ln(1024 * 0.6072)}{\ln 10}$$

$$= (\ln(out) + 6.4325).\frac{1}{2.3025} \quad \ldots\ldots\ldots (1)$$

3.1 Direct Digital Synthesizer based on CORDIC algorithm.

The direct digital synthesizer (DDS) based on LUT architecture deployed in the simulation of FFT spectrum analyzer is based on two principles: 1. an optimized Coordinate Rotation Digital Computer (CORDIC) algorithm is implemented for phase to sine amplitude conversion [3]. This algorithm proposed utilizes dynamic transformation rather than static ROM addressing. 2. Taylor series approximation. The DDS is executed in rotation mode.

The digital generation of sine wave requires two operators based on the conventional CORDIC algorithm. A digital phase accumulator is put into use to increment a constant phase in each cycle of the system clock. In this system, the output frequency is the function of clock frequency fCLK, the length (in bits) of the phase accumulator "N" and the phase increment "Δθ". The output frequency is defined by following equation 2 [3].

$$f_{OUT} = \frac{f_{CLK} * \Delta\theta}{2^N} Hz \ldots\ldots\ldots (2)$$

The output of the phase accumulator is saw-toothed waveforms that signify the linearly changing phase of a sinusoidal signal.

The CORDIC architecture implements the elementary rotations requiring only shift and add operations to generate the sine and cosine functions. It is alternatively termed as CORIDC based look-up table rotator. It undergoes few rotations before a phase shift of 90 degrees. A selector aids in performing the phase to complex sinusoid conversion. Refer Fig.2

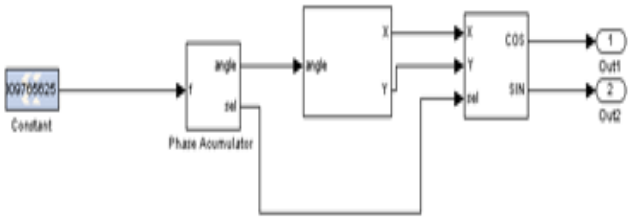

Fig.2. DDS based on CORDIC algorithm subsystem implemented in Simulink

The DDS utilizes fewer slices and LUTs as compared with traditional ROM based ones.

3.2 Filters

The mixer block is followed by decimation filter. The decimation filter implemented in the FFT spectral analysis is half - band decimation FIR filter. The filter design is achieved by using FDATool in MATLAB Simulink, Xilinx System Generator. The FDAToolaids to design the filter by indicating the windowing function, number of singed bits and binary ports. Hamming or Hanning window function is put in operation considering better efficiency. The co-efficient thus obtained is shifted to workspace using "NUM" function to

verify the required filter obtained before it is being saved in a .fda format. Finally it's implemented in a multiply and accumulate FIR block available in Simulink. The function used for implementing the same is xlfda_numerator ("FDATool"). The FIR digital filter thus obtained is in a cascaded pattern. Refer Fig 2 [10].

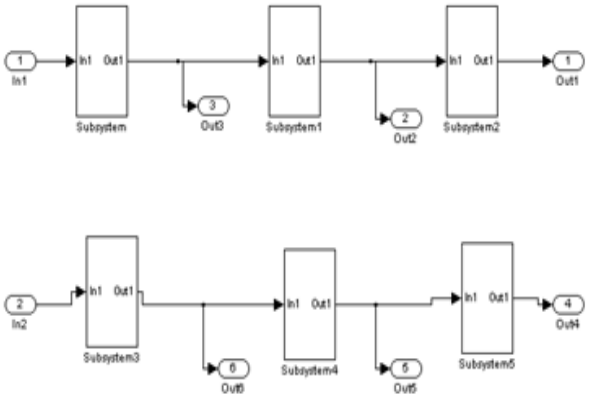

Fig.2. FIR filter implemented using FDATool in Simulink

FIR filter is replaced by Goertzel filter and tested as a part of betterment of the device. The output of the filter depends on the windowing factor and transfer function implemented. A second order recursive Goertzel filter is implemented which computes Fourier co-efficient such that it is less than one signal period. Therefore, a faster detection time is accomplished when the greatest common divisor of the input signal frequency is small. It is less prone to numerical overflow problem in case of fixed point arithmetic implementation. The algorithm is best suited for time varying sinusoidal analysis [6]. It occupies less number of slices and loop-up tables as compared to finite impulse response filers. It aids in extracting the amplitude component of the signal thus giving enhanced FFT spectral analysis and superior bandwidth resolution. The Goertzel filter is deployed in a cascaded mode.Fig 3.

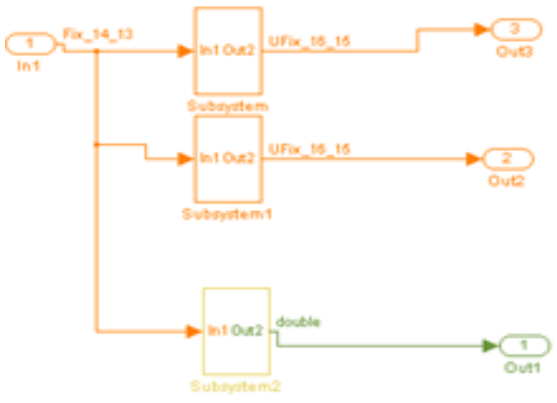

Fig.3. Goertzel filter implemented in Simulink

The frequency resolution of the windowed signal is restricted by the width of the central lobe of the window spectrum. Consequently, the ability to distinguish two closely spaced frequency components amplifies as the main lobe of the window gets tapered. As the central lobe narrows and spectral resolution improves, the window energy spreads into its side lobes, and spectral leakage deteriorates. In general, there is an exchange of amid leakage suppression and spectral resolution. Thus efficient and suitable windowing function is selected based on the below mentioned table characteristics. (Table 1)

Table.1. Characteristics of Window Functions

Window	-3dB Main Lb Width	-6 dB Main Lb Width	Max Side Lb	Roll-Off(dB/decade)
Uniform	0.89	1.21	-13	20
Hanning	1.44	2.00	-31	60
Hamming	1.30	1.82	-43	20
Blackman-Harris	1.62	2.27	-71	20
Blackman	1.64	2.30	-58	60
Flat Top	3.72	4.58	-93	20

Hamming and Hanning windows were chosen based on the requirement parameters and effective spectral analysis.An FFT generates a discrete frequency spectrum. The continuous, periodic frequency spectrum is sampled by the FFT, just as the time-domain signal was sampled by the ADC

3.3 Fast Fourier Transform (FFT)

The spectrum analyzer uses FFT to obtain the spectrum components of the signal. Decimation in time radix-2 with 1024 sample points FFT algorithm is executed in this project. It divides up the input data into short interleaved subsequences. This type of FFT can be performed using butterfly operation.

The FFT is implemented in radix 2 point algorithm in a FFT V3.2 block. The inputs, both real and imaginary parts are fed into the FFT subsystem with two delay blocks in the respective input ports. The devices supported by the FFT subsystem are Virtex-4, Virtex-II, Virtex-IIPro, Spaertan-3 and Spartan-3E.

4. Implementation in MATLAB Simulink

The subsystems for each block created in Simulink andintegrated together to obtain the FFT spectrum analyzer. The Simulink along with Xilinx System Generator provided the perfect environment for extracting the Verilog/VHDL code from the block diagram. The implementation needs several details which were verified at each stage of the integration. The 14 bit ADC available in the Simulink converts the analog input to digital signals before its being sent into a multiplexer (2*1) where digital mixing of the signal takes place. The direct digital synthesizer acts as digital mixer. The RAM used is two types, distributed memory or block memory. The digitized mixed output is a fixed point implemented value (such as fix_13_12) which indicates that the number of bits to be 13 and number of binary point to be 12. At each stage, we need to implement the fixed number of bits and binary points for correct implementation. Thus fixed point implementation is explained which is the first stage of

Xilinx system generator simulation. The FIR filter is implemented in cascaded form which reduces the magnitude of input signal spectrum. The finite impulse response filters was implemented using FDATool software according to the magnitude and impulse response required. The bandpass filter of decimation type which can be specified by the decimation factor two at each stage. This controls the bandwidth of FIR filters. The signal thus obtained is processed in RAM and ROM blocks for window function implementation. Hamming and Hanning window functions used aid in evading spectral leakage. The windowed signalthus developed passes through real and imaginary port of FFTV3.2 block. The algorithm used for implementation will be pipelined structure and radix-2 point FFT. The input spectrum is a scaled one.The values are truncated so that decimation values are not the recurring one. After the FFT stage CORDIC processor assist in obtaining the magnitude and phase response of the signal. The other CORDIC blocks implement the logarithmic module which defines the output spectrum in decibel form. The logarithmic module implemented needs additional gain block as log base 10 module is unavailable in Xilinx System Generator 8.1.

Xilinx design suite 10.1 is used for compilation of extracted verilog or VHDL code. The code is checked for syntax before it is being implemented on an FPGA device. In this interactive process, model inputs were specified and outputs were monitored and simulation was initiated for the system. The test bench generator captures the simulation results and generates a VHDL test bench for each simulation run. This test bench includes an instance of the system being modeled driven by the same inputs as the Simulink model, and the behavioral code to test that its output values are identical to those of the Simulink simulation. With these automatically generated test benches, a logic designer can detect problems with the mapping of the Simulink model to HDL and determine errors generated by the manually designed control logic.

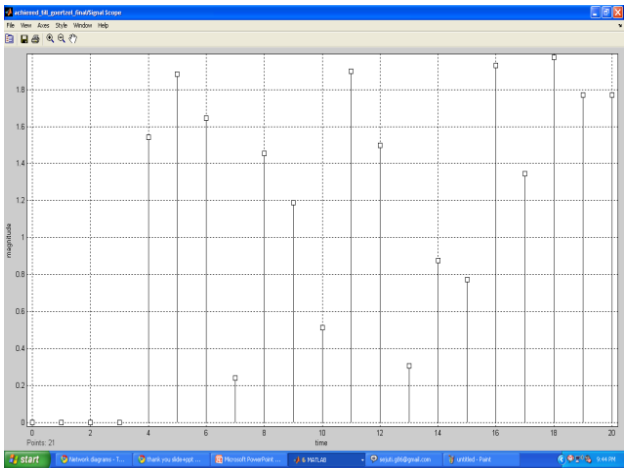

Fig.5. the Goertzel filter implemented

5. RESULTS

The FFT spectrum analyzer with FIR filter's probable magnitude and phase outputsare displayed.

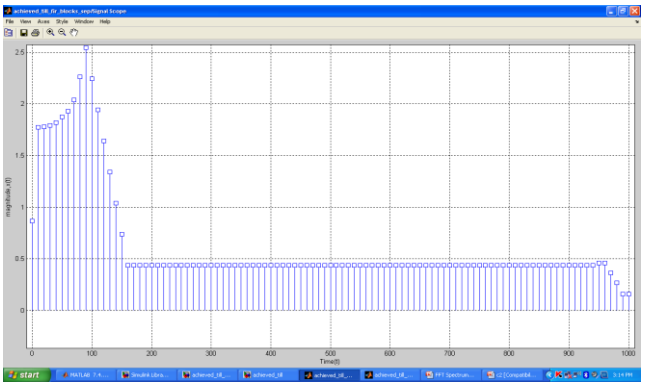

Fig.4a. FFT Magnitude output of power harmonic signal

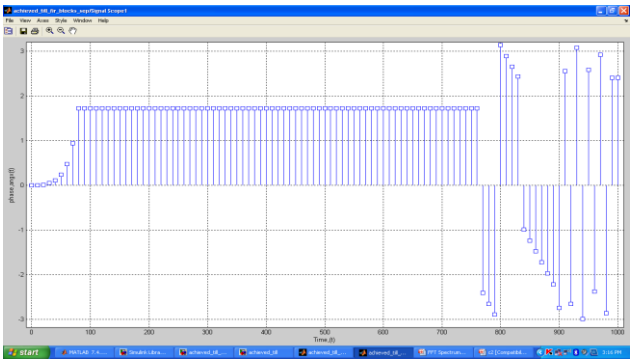

Fig.4b. FFT Phase output of power harmonic signal

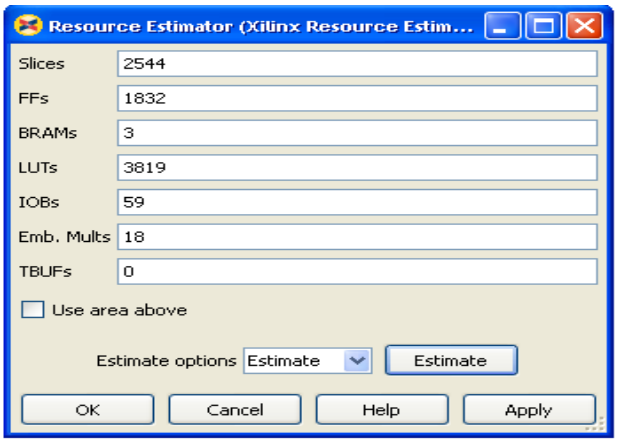

Fig.6. implemented Goertzel filter occupies less number of slices and LUTs

Fig 6 elucidates the fact that Goertzel filter implemented occupies less space (LUTs and Slices) on FPGA device [14] when integrated in the FFT spectrum analyzer. The summary derived from Resource Estimator in Xilinx System Generator (Matlab Simulink) was sustained by the same results being showcased in ISE Design suite V10.1, determining minimal

use of LUTs (11% approx of FPGA device area) as compared to the FIR filter one (40% approx FPGA device area).

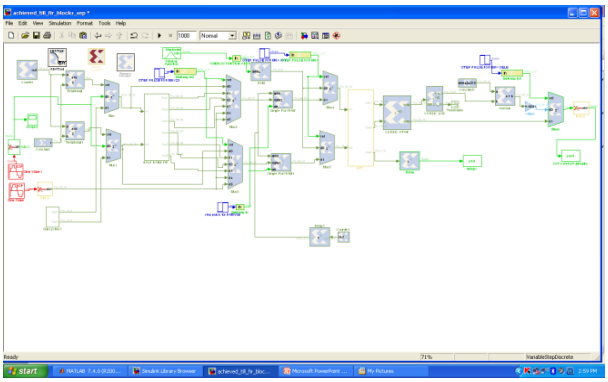

Fig.7. the whole spectrum analyzer after integrating all the subsystems:

The subsystems were integrated in a common platform Xilinx System Generator V8.1 (Matlab Simulink) and the verilog or VHDL codes were generated. The code generated in checked for syntax in ISE Design Suite 10.1 and the RTL schematic is obtained shown in fig 7. The HDL test generator is used to convert Simulink simulation results into a form that can be used to verify the behavior of FPGA hardware.

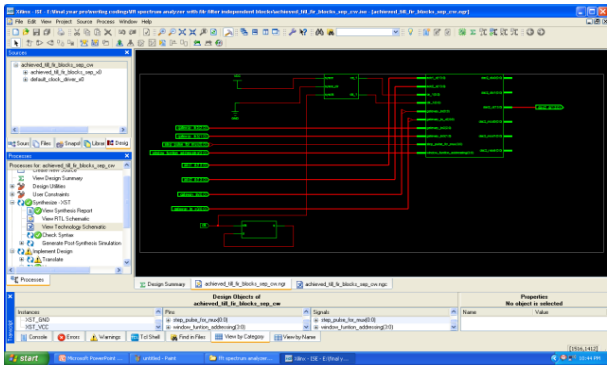

Fig.8. the RTL schematic obtained from ISE design suite 10.1:

6. CONCLUSION

We have demonstrated FFT spectrum analyzer using Goertzel filter implemented in a FPGA device which could be effectively used for analysis of power harmonics arising out of electric power transmission leading to heavy losses. The area occupied is less than the traditional FIR filter ones. It also aids in better frequency resolution, superior spectral analysis and bandwidth resolution. This analyzer can be remodeled effectively based on requirement analysis. The FFT algorithm along with Goertzel Filter will be further used to evaluate power system load variations.

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