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# Design and Simulation of Scalable Fast Parallel Counter

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## ABSTRACT
In this research paper, we report an entirely different approach to design a scalable fast parallel counter with improved performance in terms of component and transistor counts. Subsequently the simulation tests are carried out for a wide range of input conditions to validate the design. The main advantages of this scalable counter include low power consumption in milliwatt (mw) range and have speed in the range of GHz. The proposed design is modular in nature indicating that it can easily be upgraded or applied for large counters easily. Repeated use of basic building blocks such as 3-bit synchronous parallel counter, simple D flip flop and 2-bit synchronous parallel counter with enable signal made the design of counter simpler and modular. The logic uses early overflow states enabling all the blocks in the architecture concurrently at the system clock. The pipelined structures together with early overflow based logic provide correct functioning of all building blocks without ripple effects. The design is implemented using Microwind, Digital Schematics (DSCH) and 0.12 µm technologies. Performance shows a total power consumption of 0.164 mw with a clock speed of 1GHz.

## General Terms
Low Power VLSI Design, Digital Electronics, Sequential Circuits, State Equations.

## Keywords
Early Overflow State, Counter Width, Counting Path, State Look-Ahead Logic, Digital Circuits, Chip Area.

## 1. INTRODUCTION
Counters are used in almost all digital circuit and systems such as frequency synthesizer, measuring systems, analogue to digital converterss and a wide range of circuits used in communication systems [1]. Counters are also used as basic building blocks for more advanced digital logic circuits [2], [3]. High speed parallel counters find numerous applications for arithmetic operations that include neural networks and triggering the nuclear instruments [3], [4]. The key features required will vary greatly depending upon a particular application. In some cases we require counters with long counting width and high count frequency. It is highly desirable that counters must be designed in such a way that they are independent of counting width and yet in other cases, synchronous high speed parallel counters are very much in demand [5]. While designing fast counters, it is a big challenge that wide and fast counters will result in much increased chip area since speed and area increase simultaneously [6]. The desirable and important key features of counters implemented at VLSI scale include relatively constant counting time with increased counting speed, digital output and stable VLSI implementation [7]. Many journals have reported different counters with large counting width that have been designed and implemented by researchers [8], [9]. Mostly these designs have used concept of enabling higher order blocks and ANDing of the overflow states of lower order blocks which have ultimately resulted in increased complexity of design. The designs have poorly performed on counter frequency requirements [1], [2]. These limitations have been guiding force for a better an improved design as proposed in this paper.

## 2. FAST MODULAR COUNTER DESIGN
We present the main architecture of a modular and scalable counter with high speed and high clock frequency in this section. First, a representative block diagram is proposed and then the main architecture is proposed with analysis of its performance.

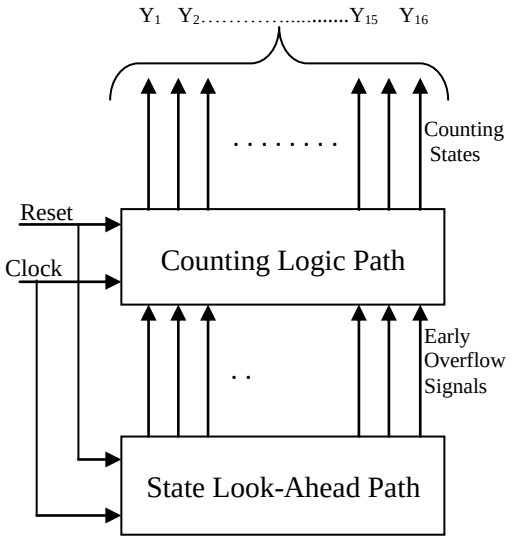


**Fig 1 : Block diagram of fast-scalable-parallel counter**

### 2.1 Block Diagram
The block diagram of scalable high speed parallel counter for 16-bit width is represented by figure 1. As shown in the figure 1, the counting path circuit consists of synchronous 3-bit parallel counter, pipelining structure consisting of simple D-flip flop and synchronous 2-bit parallel counter respectively in the sequence. The state look-ahead path consist of 3-input AND gates and inverters. Counting path logic performs counting of states while the state look-ahead logic circuit

indicates early overflow signals which are required by the counting path for proper working of the counter. A common clock and reset signals are connected to both paths which finally results in a synchronous working type of counter [8].

overflow states in the state look-ahead path circuit. Depending upon the number of output bits of BLK1, the overall width of the counter can be increased to any number of bits.

Circuit diagram of circuit block BLK2 is shown in figure 4. It

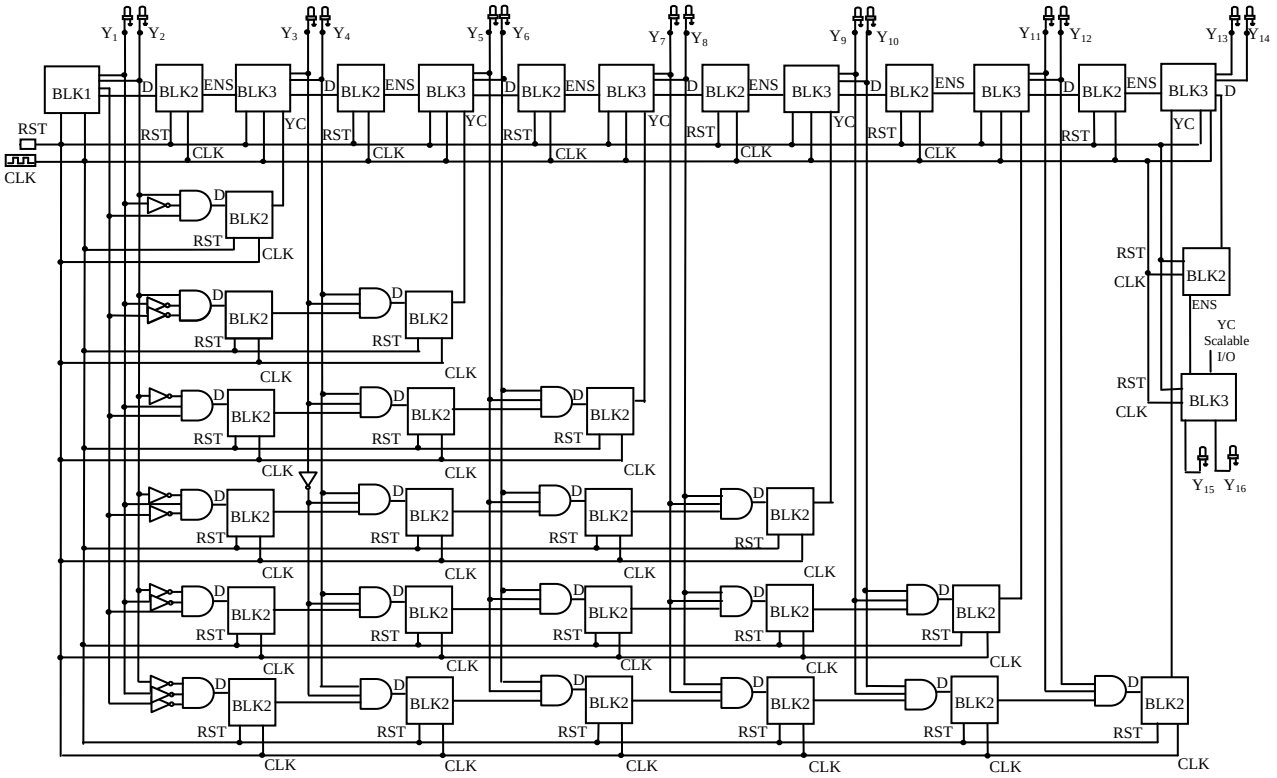


**Fig 2 : Overall architecture of 16-bit sacalable high speed parallel counter**

## 2.2 Design of Architecture

The architecture of scalable high-speed parallel counter for 16-bit counter width is shown in figure 2. The figure 2 clearly shows the counting path which consists of three different circuit blocks as indicated by labels of BLK1, BLK2 and BLK3. The BLK2 is acting as a pipelining structure between BLK1 and BLK3 and then subsequently between successive BLK3s. In the state look-ahead path, each states of BLK1 are selected and then subsequently pipelined. This is used for enabling the BLK3s and the level of pipelining is depending upon the BLK3's position in the counting path. In state look-ahead path, the left most columns, consisting of inverters, 3-bit input AND Gates and BLK2s show the selection and pipelining of early overflow states of BLK1. And the successive columns in the state look-ahead path show the ANDing of the selected pipelined states with the overflow states of the BLK3s coming to the corresponding positions in the counting path. For enabling $i^{th}$ BLK3 in the counting path, we need to generate the enabling signal from state look-ahead path up to the $(i-1)^{th}$ BLK3.

A detailed circuit diagram of circuit block BLK1 is separately shown in figure 3. It is a synchronous 3-bit parallel counter. From BLK1, outputs $Q_0$ & $Q_1$ are taken directly as the LSBs and an additional output EN1 is also generated from this circuit which is used as enabling signal subsequently. The EN1 signal is given as the input to the circuit block BLK2. All the three outputs of BLK1 are used for the selection of early

is a simple D flip-flop and it acts as a delay element in the circuit. BLK2 is used in both the counting path and state look-ahead path. In counting path the output of BLK2 is given as the block circuit enabling signal ENS to BLK3. Thus it can be seen that in counting path, BLK2 is pipelining the enable signals of BLK3s and in state look-ahead path, pipelining the early overflow states.

Circuit diagram of BLK3 is shown in figure 5. It is a synchronous 2-bit parallel counter. BLK3 produces its outputs $Q_0$ & $Q_1$, which forms the MSBs of the counter. Also an additional output EN3 is generated by ANDing it's outputs $Q_0$ and $Q_1$ with the YC signal, which is generated by the state look-ahead path. The signal EN3 is pipelined again by BLK2 and is given as the input ENS to the next block. The overflow states of each block are predetermined and the output states of BLK1 are decoded, in other words it means selecting a particular output state to enable a particular circuit block by the addition of appropriate number of delay elements. The state look-ahead path circuit selects different states of BLK1 and then introduces suitable delays or pipelines those states depending upon the order of BLK3s in the counting path. For this the enable supporting signals are required to be generated. To enable the highest order blocks in the counter design, the repeated delaying and performing ANDing operations of the selected states of BLK1 are required.

# 3. CIRCUIT OPERATION

The entire circuit operation of counting can be explained by using the concept of counter state equations. The state equations are explained in the following section.

## 3.1 State Equations

By using early overflow pipelining equations, the counter state equations can be easily derived. It is known that for enabling the count states $Y_{16}$ and $Y_{15}$ which are current count states, the state equation must contain $y_{14}$, $y_{13}$,...$y_1$ which are the past count states. We have derived 16-bit state equations by starting from 4-bit counter state equations.

$$Y_4Y_3Y_2Y_1 = Y_4Y_3 pipelined\ (y_{1\text{-}2}\,\tilde{y}_{1\text{-}1}) \quad (1)$$

Here the 3-bit outputs of BLK1 are represented by $y_{1\text{-}3}$, $y_{1\text{-}2}$, and $y_{1\text{-}1}$. Even though 3-bits are available only last two LSBs are taken into account for the 16-bit counting operation. Next 6-bit counter state equations can be given as -

$$Y_6Y_5Y_4Y_3Y_2Y_1 = Y_6Y_5 pipelined\ [(y_4y_3) pipelined (y_{1\text{-}3}\tilde{y}_{1\text{-}2}y_{1\text{-}1})] \quad (2)$$

For an 8- bit counter state equations may be given by -

$$Y_8Y_7Y_6Y_5Y_4Y_3Y_2Y_1 = Y_8Y_7 pipelined\ [(y_6y_5)\ pipelined\ [(y_4y_3)\ pipelined\ (y_{1\text{-}3}\tilde{y}_{1\text{-}2}\,\tilde{y}_{1\text{-}1})]]. \quad (3)$$

For 10-bit counter state equation are given as follows-

$$Y_{10}Y_9Y_8Y_7Y_6Y_5Y_4Y_3Y_2Y_1 = Y_{10}Y_9 pipelined\ [(y_8y_7)\ pipelined\ [(y_6y_5)\ pipelined\ [(y_4y_3)\ pipelined\ (\tilde{y}_{1\text{-}3}\,y_{1\text{-}2}\,y_{1\text{-}1})]]]. \quad (4)$$

For a 12-bit or even higher bit counter, the state equations use count state $y_4\,\tilde{y}_3$ of first block circuit BLK3 instead of its overflow states given by $y_4y_3$. Thus we can write further counter state equations. For 12-bit the state equations are-

$$Y_{12}Y_{11}Y_{10}Y_9Y_8Y_7Y_6Y_5Y_4Y_3Y_2Y_1 = Y_{12}Y_{11} pipelined\ [(y_{10}y_9)\ pipelined\ [(y_8y_7)\ pipelined\ [(y_6y_5)\ pipelined\ [(y_4\,\tilde{y}_3)\ pipelined\ ()]]]] \quad (5)$$

Similarly for 14-bit counter state equations are given by –

$$Y_{14}Y_{13}Y_{12}Y_{11}Y_{10}Y_9Y_8Y_7Y_6Y_5Y_4Y_3Y_2Y_1 = Y_{14}Y_{13} pipelined\ [(y_{12}y_{11})\ pipelined\ [(y_{10}y_9)\ pipelined\ [(y_8y_7)\ pipelined\ [(y_6y_5)\ pipelined\ [(y_4\,\tilde{y}_3)\ pipelined\ (\tilde{y}_{1\text{-}3}\,\tilde{y}_{1\text{-}2}y_{1\text{-}1})]]]]]. \quad (6)$$

And finally for 16-bit counter state equations are given by –

$$Y_{16}Y_{15}Y_{14}Y_{13}Y_{12}Y_{11}Y_{10}Y_9Y_8Y_7Y_6Y_5Y_{4\tilde{a}\tilde{y}}Y_3Y_2Y_1 = Y_{16}Y_{15} pipelined\ [(y_{14}y_{13})\ pipelined\ [(y_{12}y_{11})\ pipelined\ [(y_{10}y_9)\ pipelined\ [(y_8y_7)\ pipelined\ [(y_4\,\tilde{y}_3)\ pipelined\ (\tilde{y}_{1\text{-}3}\,\tilde{y}_{1\text{-}2}\,\tilde{y}_{1\text{-}1})]]]]] \quad (7)$$

## 3.2 Design of Clock

For proper working, path delays of counting path and state look-ahead path should be less than the clock period of the counter [1]. Here assuming that access time for both BLK1 and BLK3 are essentially equal. Let $T_{clock}$ be the clock period of the counter, $T_{Block}$ be the access time of block circuits BLK1 or BLK3, $T_{3\text{-}AND}$ be the gate delay of 3-input AND gate, $T_{s\text{-}h}$ be the combined set-up time and hold time of D flip-flop, then the following condition for $T_{clock}$ must be satisfied -

$$T_{clock} > T_{Block} + T_{3\text{-}AND} + T_{s\text{-}h} \quad (8)$$

The clock period mainly depends on the block access time. Hence, for any changes in the design like increasing the number of output bits of the blocks or using different D flip-flops the clock period will change substantially. This conditions is very stringent and must be kept in mind while designing the circuits or block for fast counters [10], [11]. In this research work, clock is designed while keeping various delays in mind.

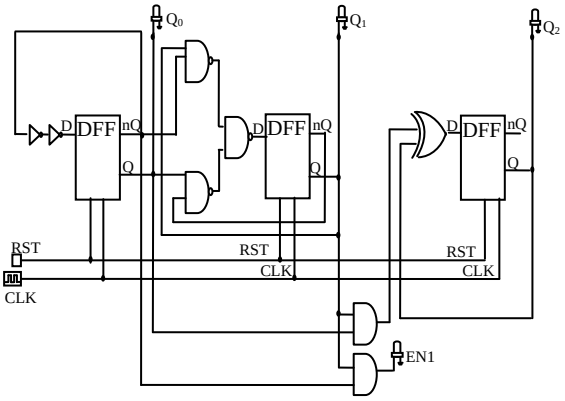


**Fig 3 : Synchronous 3-bit parallel counter**

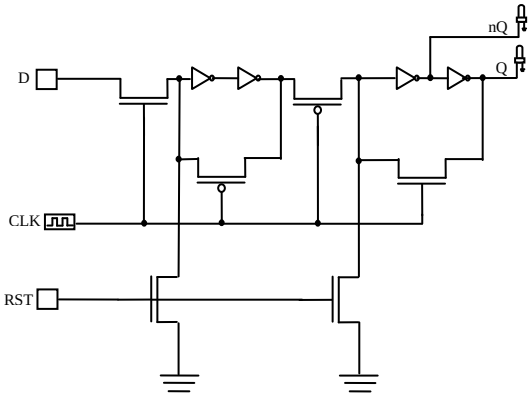


**Fig 4 : Delay element using D flip flop**

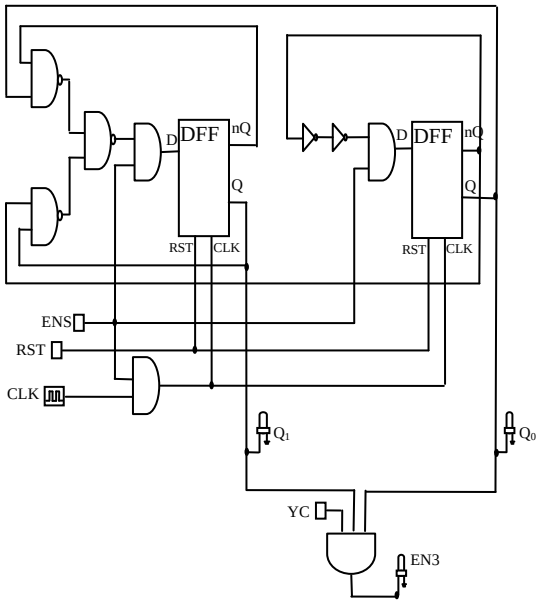


**Fig 5: Synchronous 2-bit parallel counter**

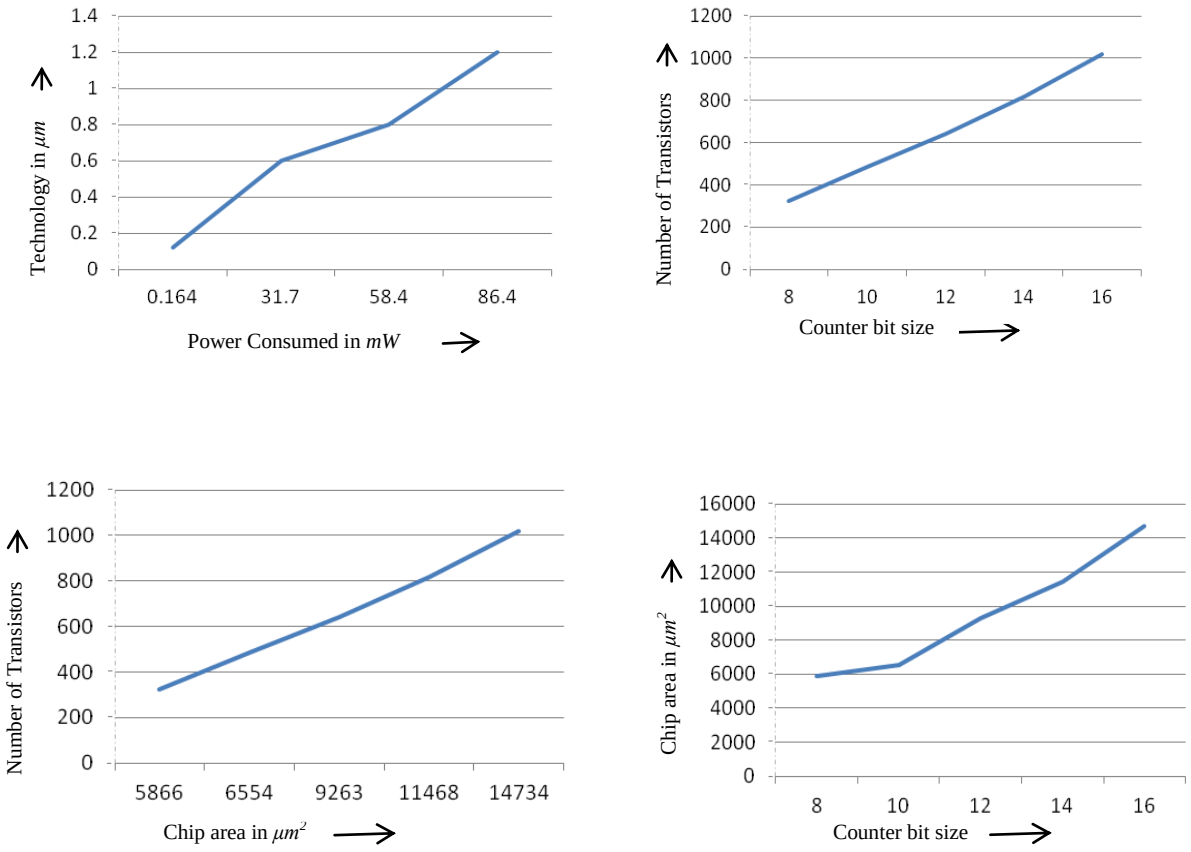


**Fig 6: Simulated results in terms of technology, transistor count and chip area utilization**

## 4. SIMULATION RESULT ANALYSIS

The performance of the scalable high-speed parallel counter is verified by simulating the circuit with wide range of input conditions. The tools used for carrying out simulation tests are mainly based on software from Microwind and Digital Schematic (DSCH) [9]. Microwind is Electronic Design Automation (EDA) software which integrates very conveniently the front-end and back-end of the chip design principles of VLSI. It is possible to generate the layout of the circuit in Microwind either by using Verilog code files of circuit design or by directly entering schematic layout. The later needs cross checking of any violation of design rules. It is also possible to measure the area utilized by the circuit design by using Microwind software. During this research DSCH is mainly used for the design of circuit schematics and for generating timing waveform diagrams.

**Table 1. Supply voltage and power consumption vs. technologies for 16-bit counter**

| Technology | Supply voltage | Power |
|---|---|---|
| 0.12µm | 1.2V and 2.5V | 0.164 mW |
| 0.6 µm | 5V | 31.700 mW |
| 0.8 µm | 5V | 58.461 mW |
| 1.2 µm | 5V | 86.401 mW |

### 4.1 Power Estimation

We simulated a 16-bit scalable parallel counter circuit which was designed using Microwind 3.1. It produced encouraging results. The clock frequency of 1 GHz is chosen for the simulation test and verifications. The total power consumed by the counter circuit under different technologies is compiled in Table 1. For 0.12µm (equivalent to 120 nm technology) technology, the power consumption is at the minimum value of 0.164 *mW* as seen in Table 1. As for the other technologies, the power consumption increases with increasing size of the technology. The supply voltage for the various technologies is shown in second column. For 0.12 µm technology power supply is selected as 1.2 volts and 2.5 volts and for all other technologies it is 5 volts.

**Table 2. Components and transistors counts for 16-bit counter and its subsystems**

| Component | Number of Components | Transistors per Component | Total Transistor |
|---|---|---|---|
| BLK1 | 1 | 70 | 70 |
| BLK2 | 28 | 14 | 392 |
| BLK3 | 7 | 58 | 406 |
| 3-input AND Gate | 21 | 6 | 126 |
| Inverter | 12 | 2 | 24 |
| Total (for complete 16-bit counter) | | | 1018 |

**Table 3. Transistor count and area requirement on chip for different bit sized counters**

| Counter bit size | Transistor count | Area ($\mu m^2$) |
|---|---|---|
| 8 | 322 | 5866 |
| 10 | 486 | 6554.9 |
| 12 | 644 | 9263.7 |
| 14 | 820 | 11468.5 |
| 16 | 1018 | 14734.5 |

## 4.2 Transistor Count and Area Estimation

The simulation results of a 16-bit counter for its transistor performance. All other results are graphically summarized in figure 6 for quick visual interpretation.

## 4.3 Timing Waveform Diagram Analysis

The timing waveform diagram of simulation tests of the scalable high-speed parallel counter is shown in the figure 7. It has been clearly observed that there are fluctuations in timing waveforms of the counter at various levels of the signals. From the figure 7 it can also be clearly observed that the least significant bits are subjected to more fluctuations compared to the most significant bits.

The LSB $Y_1$ has the frequency of *CLK/2*. The $Y_2$ has the frequency of *CLK/4* and so on. Thus in the counter itself we can find signals with different frequencies which are below

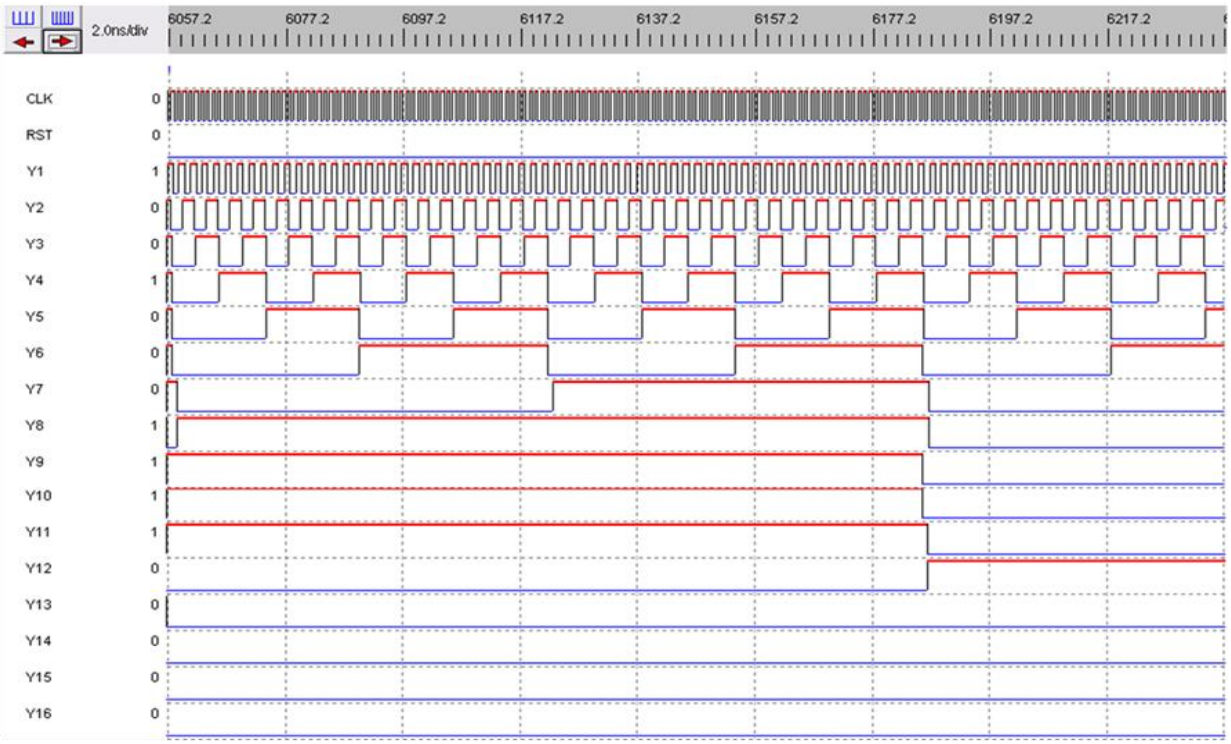


**Fig 7: Timing Diagram of 16-bit counter**

count are shown in Table 2. The number of transistors used by each block and also by the logic gates and inverters are shown there in. It includes that of the circuits for the state look-ahead path. A total of 1018 transistors have been used in implementing the counter. Table 3 shows the total number of transistors for various bit sized counters i.e. counters of size varying from 8-bit to 16-bit and corresponding chip area requirements. We analyzed area utilization criterion for 0.12µm Technology. After analyzing the increase in transistor count with increase in counter bit size, we concluded that there is approximately 1.28 times of increase in transistor count and approximately 1.26 times increase in area for each 2 bit increment of counter bit size. Also it became evident from analysis that since the counter design consists of more number of D flip flops, we can further reduce chip area requirements by using advanced D flip flops with much less transistor count and thereby improving overall design

that of the clock frequency. As it can be seen in figure 6, the counting state at the beginning of the counter is set to an arbitrary example value of *[0 0 0 0 0 1 1 1 0 1 1 1 1 1 0 1 0]*. The subsequent counting can be easily verified from the waveforms.

We simulated the 16-bit circuit with constant clock frequency of 1GHz for various technologies. Table 1 show the variation in power for various technology used while simulating the tests. From the Table 1, it can be verified that while designing at lower technology values (reducing the size of channel length) there can be considerable reduction in power consumption. Our simulation results show that if the technology used is reduced in size by a factor of 10, the power consumption reduces by a factor of roughly over 500 times. The power consumption initially reduces with a slow rate, but as the technology size reduces further the power consumption reduces exponentially faster and faster. Our simulation results are carried out on an average accuracy software and hardware,

which may have large errors but a clear trend of power reduction is observed. It has become evident that with more precise experiments and simulation tests, the accuracy of the tests can further improve. Also as indicated earlier that advanced and improved D flip flops may result in much more reduction in transistor count and lower power consumption.

## 5. CONCLUSTION

In this paper we have reported the concluding analysis and results of our simulated design and verifications on a scalable high-speed parallel counter. We have subsequently tested and verified design starting from 8-bit to 16-bit count size. The special features of this counter design which have emerged out of testing and verification process include the modularity and pipelining structure. One can implement counter of any larger numbered bit size without needing much complexity and design efforts due to the nature of the modularity of design. To achieve this, we only need to have added BLK3 and BLK2 in appropriate numbers at appropriate positions in order to design a desired larger bit width counter. Positioning of BLK2 (D flip-flops) has much more bearing in the counter design and subsequently its performance. The introduction of BLK2 has resulted in exclusion of AND gates with large fan-in for the enabling of higher order count bits. This is clearly observed as an advantage. After attaining the maximum count of a given design, if it is required to further increase the counter width, it can be done simply by increasing the counter width of BLK1. Since all the circuit blocks except BLK1, of counting path are preceded by BLK2 (D flip flop), therefore, all the circuit blocks will be getting enabled with constant delay. Hence there is no mismatch of delays. Since the counter is having binary output, there is no need of any detector circuits at output. The result analysis shows some of the important findings in terms of transistor count and chip area requirements. The transistor counts have shown very comparable results available for literature review. Some rough patterns have emerging for the possible relationship between transistor count, power consumption and technology size.

These findings may result in very concrete physical laws and principles if verified with higher precision and accuracy involved with the software tools used for implementation. The future work will involve further refining the results and improved designs of more complex circuits and systems.

## 6. ACKNOWLEDGEMENT

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