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A Physics–based Model for Electrical Parameters of Double gate Hetero-material Nano Scale Tunnel FET

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ABSTRACT
This paper focuses a hetero gate material dielectric DG TFET with low band gap source material, which offers high I_{on} / I_{off} ratio, sub 60mV/dec subthreshold swing along with significant improvement in on current. Here analytical model for 2D electric field is derived from Poisson's equation and is used to determine the subthreshold swing, transconductance, output conductance, gate threshold voltage, and drain threshold voltage of the proposed device. The results of derived model are compared with that of simulated results to examine the validity of model of electrical parameters and also comparison of the analytical model results with simulated results shows excellent agreement.

General Terms
Modeling, simulation.

Keywords
Band-to-band tunneling, hetero material, subthreshold swing, threshold voltage.

1. INTRODUCTION
MOSFETS are scaled down to achieve higher packing density, higher on current etc. However, the subthreshold swing can not be scaled. As a result, it becomes difficult to turn off the device and reduces the noise margin. As such, it becomes more vulnerable to noise [1]. At the same time, in order to maintain a high on current with reduced off state leakage, a reduction of subthreshold swing is necessary and has become one of the most important technological issues. MOSFETS are based on drift and diffusion mode of carrier transport where subthreshold swing depends on thermal voltage and at the least it can be $\geq$ 60 mV/dec. Therefore one needs to design a device which uses other mode of carrier transport so that a lower subthreshold can be achieved. The other modes are based on impact ionization [2] and interband tunneling [3]. Sub 60mV/decade value of subthreshold swing is possible for these two modes of carrier transport [4]. The impact ionization MOSFET appeared to be very promising due to its near ideal switching characteristics [5]. But problems like threshold voltage shift caused by hot carrier injection, non-rail to rail voltage swings, and high operating voltage requirements will arise in Impact ionization MOSFETS [6]. However, devices based on these mechanisms fail to meet the ITRS requirements [7].

This paper presents a Tunnel FET which is based on interband tunneling [8]. Tunneling current is a quantum mechanical effect that shows exponential dependence on tunnel width. The on current in case of silicon tunnel FET is 10 μA/μm, which is two orders of magnitude lower than the ITRS requirement [9]. It can be stated that lowering the tunneling gap can be a way to overcome the on current limitation [10]. In order to meet the ITRS requirement, it has been proposed to use double gate technology in conjunction with hetero gate dielectric. The double gate tunnel FET is based on band-to-band tunneling.

In this paper we have derived the drain current on the basis of Poisson's equation and Kane's generation rate model. As such no model has been derived for threshold voltage of tunnel FET. Threshold voltage is one of the most important electrical parameter of tunnel FET [11]. It is already established that unlike MOSFET, there are two threshold voltages for tunnel FET i.e. gate threshold voltage and drain threshold voltage [11]. In MOSFETs, the threshold voltage is defined at the onset of strong inversion. But in Tunnel FETs, the definition of threshold voltage is completely different and threshold voltage is the voltage at which drain current changes from quasi exponential to linear. Moreover, the energy barrier narrowing in tunneling current is a complex functions of both gate and drain voltage. Gate threshold voltage and drain threshold voltages are analytically derived first time considering conductance change method.

2. DEVICE STRUCTURE AND OPTIMIZATION
The structure of the proposed device is as shown in figure 1. The basic structure is a p-i-n double gate device operating under reverse bias condition. It can operate both in n and p channel modes [3]. In p mode, $V_{GS} < V_F$ and in n mode, $V_{GS} > V_F$, where V_F is a reference voltage required to align the P^+ valence band and channel conduction band. In n-channel mode, tunneling occurs in the source side while in p-channel mode, tunneling occurs in the drain side. An electron inversion layer is created in the channel at the interface with the gate dielectric when a gate voltage greater V_F is applied. Tunneling takes place from the source valence band to the conduction band in the inversion layer of the channel [12]. As mentioned, we have used heterogate dielectric. A low-K gate oxide at the drain side and high-K oxide at the tunneling junction are used. To reduce the ambipolar current at the drain side, low-K gate oxide is used.

Figures 2 and 3 show the band diagram of the n-channel TFET in the ON and OFF states. In the OFF state, the potential barrier between the source and channel is so wide that no tunneling occurs even though a very small leakage current exists. In the on state, when the gate voltage exceeds the threshold voltage the potential barrier between the source and channel becomes narrower and a significant tunneling current flows [13].

Ambipolar current is defined at $V_{GS} = -0.1\,\text{V}$ and $V_{DS} = 0.7\text{V}$. In a conventional TFET, as the thickness of the oxide layer is decreased, the tunneling current from gate starts flowing. This not only adversely affects the device performance but also increases the standby power of a VLSI chip. To decrease the effective oxide thickness (EOT) at the tunnel junction, high-K gate oxide is used so that the gate leakage, i.e. the gate tunneling current is reduced [14]. N^+ polysilicon gate material is used as gate electrode with work function 4.5eV. The low-K gate oxide with relative permittivity 3.9 and high-K gate oxide with relative permittivity 25 are used here. In the source side, a low band gap material (germanium) is used to increase the tunneling probability as tunneling probability is a function of band gap E_g [15]. The tunneling probability is calculated by Wentzel-Kramers-Brillouin (WKB) method [15]. The bandgap of monocrystalline Ge is 0.66 eV and that of poly-Ge has a high density of defects with associated trap state energy level located ~ 0.1eV away from the valence-band edge, [16], which would effectively lower the tunnel bandgap. To operate this device, source is grounded, 1.5 V is applied to the gates, and drain is connected to 0.7V. As the gate voltage increases above V_F , the bands in the intrinsic region are pushed down in energy, narrowing the tunneling barrier and allowing tunneling current to flow.

3. ANALYTICAL MODELLING

3.1 Modeling for electric field and tunnel current

The analytical model for proposed device has been derived solving 2D Poisson's equation in the channel and source, and 1D Poisson's equation in the drain.

The analytical model for electric field, tunneling current, subthreshold swing, transconductance, output conductance, gate and drain threshold voltages are derived. The following assumptions are made while deriving the model for the proposed device.

(a) The source/ channel and drain/channel depletion regions are free from mobile charge.
(b) Trap charges are considered as zero.
(c) The surface potential at the source end is considered as equal to the difference in Fermi level of P+ source and intrinsic Fermi Level.
(d) The potential drop in the depletion region of source is negligible and potential in the source region is assumed uniform and
(e) In the drain side, 1D Poisson's equation is considered to be applicable because vertical electric field is almost negligible compare to source side.

In the channel, the 2D Poisson's equation is given by [17]

$$\frac{\partial^2\psi}{\partial^2 x} + \frac{\partial^2\psi}{\partial^2 y} = \frac{qN_A}{\varepsilon} \qquad (1)$$

Where ψ is the potential, N_A is the acceptor concentration in the channel, and ε is the permittivity of the medium. In our case, the corresponding boundary conditions are

$$\begin{aligned} &\psi(x,0) = \psi_s(x) \\ &\frac{d\psi(x,t_s)}{dy} = -\frac{\varepsilon^* \{\psi_s(x) - v\}}{\varepsilon\tau} \\ &\frac{d\psi(x,0)}{dy} = \frac{\varepsilon^* \{\psi_s(x) - v\}}{\varepsilon\tau} \end{aligned} \qquad (2)$$

where v is the difference between V_{GS} and flat band voltage V_{FB} , $\varepsilon*$ is the gate oxide dielectric constant, τ is the oxide thickness, and t_s is the body layer thickness.

Solution of (1) is given by considering parabolic approximation of potential [18], given by

$$\psi(x,y) = a_0(x) + a_1(x)y + a_2(x)y^2 \qquad (3)$$

Where the coefficients $a_0(x)$, $a_1(x)$, and $a_2(x)$ are determined from this solution under the boundary conditions given in (2). Using these coefficient values, the surface potential can be found as

$$\frac{\partial^2\psi_s}{\partial x^2} - p^2\psi_s = p^2\psi_k \qquad (4)$$

where $p^2 = \varepsilon*/(\varepsilon\tau t_s)$. The surface potential is given

$$\psi_s(x) = B\exp(px) + C\exp(-px) + \psi_K \qquad (5)$$

where ψ_K is the 1-D surface potential and B and C are constants. For drain side, Poisson's equation can be approximated as

$$\frac{d^2\psi(x)}{dx^2} = -\frac{qN_D}{\varepsilon} \qquad (6)$$

where N_D is donor concentration of the drain region. Using(6), we get

$$\psi(x) = -\frac{qN_D}{\varepsilon}\frac{x^2}{2} + C_1x + C_2 \qquad (7)$$

where C_1 and C_2 are integration constants. Considering continuity of the electric field and surface potential at $x = L_1$, the constants B, C, C_1, and C_2 can be determined as

$$B = \frac{1}{K}\left\{\begin{aligned} &2\left(-\psi_k - \frac{qN_D L_1^2}{2\varepsilon}\right)\sinh p(L_2 - L_3) - 2(\phi_1 - \psi_k) \\ &-L_1 p(\phi_1 - \psi_k)e^{-p(L_1 - L_2)} + q\frac{N_D L_1^2}{\varepsilon}e^{p(L_2 - L_3)} \\ &+2(\phi_2 + V_{DS} - \psi_k)\sinh p(L_3 - L_1) \end{aligned}\right\}$$

$$C = \frac{(\phi_2 + V_{DS} - \psi_k)e^{pL_3} - e^{pL_2}(\phi_1 - \psi_k)}{K}$$

$$C_1 = \frac{1}{K}\begin{Bmatrix} 2p(\phi_1 - \psi_k)\cosh p(L_2 - L_1) - \dfrac{2qN_D L_1 \sinh p(L_2 - L_3)}{\varepsilon} \\ -2(\phi_2 + V_{DS} - \psi_k)\, p \cosh p(L_1 - L_3) \end{Bmatrix}$$

$$C_2 = \frac{e^{-pL_2}(\phi_1 - \psi_k) - (\phi_2 + V_{DS} - \psi_k)e^{-pL_3}}{K}$$

$$K = 2\sinh p(L_2 - L_3)$$

ϕ_1 and ϕ_2 are potentials, determined considering the external potential applied at $x = 0$ and $x = L_3$. The constants are B, C, C_1, and C_2 determined in different regions of the proposed device depending on different oxide thickness, gate oxide material , and region material.

The expression for E_x *and* E_y are given

$$E_x = \frac{d\psi_s(x)}{dx} + \frac{\varepsilon^*\left\{\dfrac{d\psi_s(x)}{dx} - \upsilon\right\}}{\varepsilon\tau} y - \frac{1}{2}\frac{\varepsilon^*\left\{\dfrac{d\psi_s(x)}{dx} - \upsilon\right\}}{\varepsilon\tau\, t_s} y^2 \quad (8)$$

$$E_y = a_1(x) + 2a_2(x)y \quad (9)$$

Net electric field is,

$$E = \sqrt{E_x{}^2 + E_y{}^2} \quad (10)$$

Generation rate from Kane's model is given by [18],

$$G = AE\exp\left(-DE_g{}^{3/2}/E\right)/E_g{}^{1/2} \quad (11)$$

where E is the magnitude of electric field and E_g is the energy band gap. A and D are parameters which depend on the effective mass of valence and conduction band electrons determined from device dimensions and material parameters [19].

The expression for the drain current per unit length is given by [18],

$$I_D = q\int G dv \quad (12)$$

Where q is the electronic charge, and dv is an elementary volume in the device and drain current is obtained by numerical integration.

3.2 Subthreshold swing

The subthreshold swing (SS) of a device is defined as the change in gate to source voltage required to be applied in order to change the drain current by one decade. Using (12), the SS expressed in mV/dec can be derived as

$$\text{SS} = 2.3\left(\frac{E + A'}{E^2}\frac{dE}{dV_{GS}}\right)^{-1} \quad (13)$$

where the expression for E is given by (10) and using the same expression, and $A' = DEg^{\frac{3}{2}}$.

we obtain

$$\frac{dE}{dV_{GS}} = \begin{bmatrix} \dfrac{2\varepsilon^{*2}}{\varepsilon^2\tau^2} y^2 \left(1 + \frac{1}{4}\dfrac{y^2}{t_s{}^2} - \dfrac{y}{t_s}\right)\left(V_{GS} - V_{FB} - \dfrac{d\psi_s}{dx}\right) \\ + \dfrac{2\varepsilon^{*2}}{\varepsilon^2\tau^2}\left(1 + \dfrac{4y^2}{t_s{}^2} + \dfrac{4y}{t_s}\right)(V_{GS} - V_{FB} - \psi_s) \\ - \dfrac{\varepsilon^*}{\varepsilon\tau} y\left(2 - \dfrac{y}{t_s}\right)\dfrac{d\psi_s}{dx} \end{bmatrix} \quad (14)$$

For our device, difference of Fermi level in intrinsic channel and p+ source is near about 1eV. Hence the factor which is a function of difference of Fermi levels in source and channel is neglected. Subthreshold swing mostly depends on gate oxide thickness, source doping concentration, silicon layer thickness, flatband voltage.

3.3 Transconductance (g_m) and Gate threshold voltage (V_{TG})

Determination of threshold voltage by transconductance change (TC) method. According to this method, the threshold voltage can be defined as the gate voltage where the derivative of the transconductance reaches maximum, or, in mathematical terms, when

$$\frac{d^3 I_D}{dV_{GS}{}^3} = 0 \quad (15)$$

Or, when $\dfrac{dg_m}{dV_{GS}}$ is maximum. While deriving this we have assumed that electric field is a strong function of V_{GS} compare to E_g for the same.

$$\frac{dg_m}{dV_{GS}} = P\exp\left(-\frac{A'}{E}\right)\left[\frac{A}{E^2}\frac{dE}{dV_{GS}} + \frac{A'2}{E3} + \frac{d^2E}{dV_{GS}{}^2} - \frac{A'}{E^2}\right] \quad (16)$$

where $P = \dfrac{AqWL}{\sqrt{E_g}}$

$$\frac{d^3 I_D}{dV_{GS}{}^3} = \frac{d^3E}{dV_{GS}{}^3} + \left(1 + \frac{A'}{E^2}\right)\frac{d^2E}{dV_{GS}{}^2} + \left(\frac{A'^2}{E^4} - 2\frac{A'}{E^3}\right)\frac{dE}{dV_{GS}} + \frac{3A'^2}{E^3}$$

$$-\frac{A'}{E^2} - \frac{3A'^2}{E^4} = 0 \quad (17)$$

Analytically, the expression for threshold voltage from above equation is,

$$V_{TG} = V_{FB} + \psi_S + \frac{\varepsilon^2\tau^2}{2\varepsilon^{*2}\left(1+\frac{4y}{t_S}\right)}\left[\begin{array}{l}\frac{\varepsilon^*}{\varepsilon\tau}y\left(2-\frac{y}{t_S}\right)\psi_S - \frac{3A'^2E}{A'^2-2A'E} \\ +\frac{A'E^2+3A'}{A'^2-2A'E} \\ -\frac{\left(E^2+A'\right)E^2}{A'^2-2A'E}\left\{\frac{8\varepsilon^{*2}y}{\varepsilon^2\tau^2 t_S}\right\}\end{array}\right] \quad (18)$$

Where ψ_S is a function of V_{DS}.

3.4 Model for output conductance (g_d) and Drain threshold voltage (V_{TD}) for double gate Tunnel FET

To derive the drain threshold voltage, output conductance change (OC) method is adopted.

We know that, $N_i^2 = N_C N_V \exp\left(-\frac{E_g}{KT}\right)$ (19)

Ni is the intrinsic concentration , N_C and N_V are effective density of states located at conduction and valence band edge.

$$N = N_C \ln\left(1+\exp\frac{E_{Fn}-E_c}{KT}\right) \quad (20)$$

$$P = N_V \ln\left(1+\exp\frac{E_v-E_{Fp}}{KT}\right) \quad (21)$$

where N and P are electron and hole concentrations, E_{Fn} and E_{Pn} are quasi Fermi level of N and P type semiconductor.

Built in potential for zero biased junction is given by,

$$V_0 = \frac{E_{Fn}-E_{Fp}}{q} = Vt\ln\left[\left(e^{N/N_C}-1\right)\left(e^{P/N_V}-1\right)\right] + \frac{E_g}{q} \quad (22)$$

Where $V_t = \frac{KT}{q}$.

Actually, bandgap energy is a function of both gate and drain voltage, when the tunnel junction is reverse biased by application of gate as well as drain voltage. Since the lateral component of electric field at the tunneling junction has greater magnitude compare to the vertical component of electric field. To derive drain threshold voltage we have assumed that energy band gap is a strong function of V_{DS} compare to V_{GS}.

$$g_d = \frac{dI_D}{dV_{DS}} = -\frac{1}{2}qI_D\left(\frac{1}{E_g}+3\frac{D}{E}\right) \quad (23)$$

The drain threshold voltage is determined where $\frac{dg_d}{dV_{DS}}$ is maximum.

$$\frac{dg_d}{dV_{DS}} = \frac{1}{2}q^2 I_D\left[\frac{3}{2}\frac{1}{E_g{}^2}+\frac{9}{2}\frac{D^2}{E^2}+\frac{3D}{E_g E}\right] \quad (24)$$

Or,

$$\frac{d^3 I_D}{dV_{DS}{}^3} = 0 \quad (25)$$

The above equation gives,

$$V_{TD} = \frac{0.066eV}{q} - V_{GS} - V_0 + V_t \ln\left[\left(e^{N/N_C}-1\right)\left(e^{P/N_V}-1\right)\right] \quad (26)$$

4. Result and Discussions

In view of the present scaling trend, the analytical model is tested on 20 nm gate length, 15 nm channel length, body layer thickness $t_s = 25$ nm , oxide thickness 3 nm for SiO_2 and 2 nm for HfO_2. Length of SiO_2 is 25 nm and HfO_2 is 10 nm. The doping levels of the Tunnel FET source and drain must be carefully optimized in order to maximize on-current I_{on} and minimize off-current I_{off}. The source doping has a large effect on the on-current level, since the tunneling takes place between the source and the intrinsic region. Therefore, the highest-possible source doping level is desirable for optimized Tunnel FET behavior. A high doping level, yet still realistic in terms of a design to be fabricated. In this paper, the doping concentration of source, drain, and channel are 10^{22} , 5×10^{18} and, 10^{16} cm^{-3}, respectively. The channel is intrinsic for enhancing electron mobility. The abrupt doping profile is used here. Simulation is done using Synopsys TCAD Tools based on non local band-to-band tunneling model [20]. Band gap narrowing is activated. Doping dependent high field saturation Canali mobility model is used.

Simulation results, shown in figures 4 and 5 show I_D vs. V_{GS} characteristics of our device. Figure 6 shows the I_D vs. V_{DS} characteristics for the proposed device. As observed, when the gate lengths are decreasing the on current of the proposed device is more. This shows that with decreasing gate length, gate has better control over tunneling junction. The subthreshold swing (SS) of the TFET, in general, is not limited to 60 mV/dec because the transport mechanism is completely different from conventional MOSFET. The actual value of SS in MOSFET is much higher than 60 mV/dec which results in increased I_{off} and thus become a major concern for low standby power (LSTP) digital applications [21]. On the other hand, with reduced SS in TFET, the supply voltage may be further reduced, which leads to a reduced power consumption [22]. Our device is a heterogate dielectric to boost the on current and to achieve steeper subthreshold slope. Tunneling takes place from valence band of the P^+ source to the intrinsic channel conduction band [23]. The tunneling occurs due to the application of gate voltage which reduces tunneling gap and creates very high local electric field. The current is governed by tunneling even though the electrons from intrinsic region move toward drain by drift-diffusion mechanism.

Next, the analytical surface potential is compared with the simulated one as shown in figure 7. It is very clear that there is an excellent agreement between the model and 2D simulated data throughout the entire channel region. This shows the approximation used for 2D effect in the model is acceptable. As shown in figure 8, the simulation results show that the horizontal component of electric field E_x has the maximum value at the tunneling junction. Likewise, the vertical component E_y also has its highest magnitude near the tunneling junction (figure 9). This means that the maximum total field is near the tunneling junction. The reason for the same can be attributed to the local band bending of energy band. When the total electric field is plotted along the vertical direction, the field is found maximum near the interface of silicon/dielectric, as shown in figure 10. From this plot, it is observed that the gate has better control over these regions. Figures 8 – 10 also show the plots of the analytical electric fields given by (8) and (9). A near exact agreement between the model and simulated data has been found.

The gate length of the optimized devices for our device is varied and the corresponding SS values are plotted in figures 11. The proposed device has steeper and low subthreshold slope when it is closer to the off state $(V_{GS} \approx 0\ \mathrm{V})$, while its subthreshold slope is relatively large and less steeper when it operates near the on state $(V_{GS} = 1.5\ \mathrm{V})$. The plots shown in figure 11 use the average of these two values of the subthreshold slope. As seen, the average SS for the proposed device is 53 mV/dec for 20 nm channel length. The small mismatch between the model and the simulated data shows the model suitability for a scaled device

Next in figure 12, the transconductance for different gate lengths is measured. Lesser the gate length better is the g_m value. In general, a better capacitive coupling of the gate with the tunnel junction leads to higher g_m when the device is scaled. However, the best g_m is found at a channel length of 20 nm. Scaling benefits of devices with hetero gates can be found only upto a gate length to which the OFF state is not degraded by Zener breakdown [24]. Moreover, in order to avoid reliability problems, care should be taken for maximum electric field in the ON state [25]. Modeled data are matching with the simulated values. The ouput conductance is also determined from simulation and compared with the ananlytical model. There is a close match between the analytical and simulated values at different gate lengths, as shown in figure 13.

The most common definition of the threshold voltage of a MOSFET assumes that $\phi_S = 2\phi_F$ at threshold ,i.e. when strong inversion reached. This definition is inadequate for double gate tunnel FETs where current is due to band-to-band tunneling. In case of thin film, double gate MOSFETs also, the threshold voltage is defined considering transconductance change method because of the reason that in this case current appears following a weak inversion mechanism [26]. In TC method, the threshold voltage is the gate voltage where the derivative of transconductance reaches a maximum. The maximum of the $\frac{dg_m}{dV_G}$ curve corresponds to the formation of channel in the device. This device exhibits a single maximum, indicating that both corners and edges build up channel at the same time. For our device we have determined the threshold voltage using conductance change method. The gate threshold voltage for the proposed device is 0.8V for 20 nm gate length as determined using TC method, as shown in figure 14.

Unlike MOSFET, tunnel FET current is controlled by two threshold voltages. A certain amount of drain voltage is always required to turn on the device. The tunneling width is a complex function of both V_{GS} and V_{DS}. The drain threshold voltage has similar control over tunneling junction as that of gate threshold voltage. The drain threshold voltage is defined as the drain voltage when drain current changes from quasi exponential to linear. The method of obtaining the drain threshold voltage is also same as that of gate threshold voltage. The drain threshold voltage is determined at maximum of $\frac{dg_d}{dV_D}$. Figure 15 shows the drain threshold voltage is around 0.42 V. Comparison of modeled data and simulated gate and drain threshold voltages are observed in figure 16 and there is a small mismatch. This is due to the fact that while deriving the model for V_{TD}, we have assumed tunnel band gap is a function of V_{DS} only. However, this mismatch is within $\pm 5\%$ and analytical model results can be considered as well agreed with simulated results.

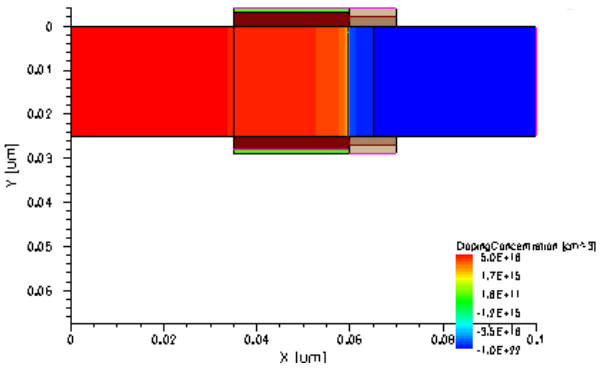


Figure 1: Hetero Double gate-dielectric Tunnel FET

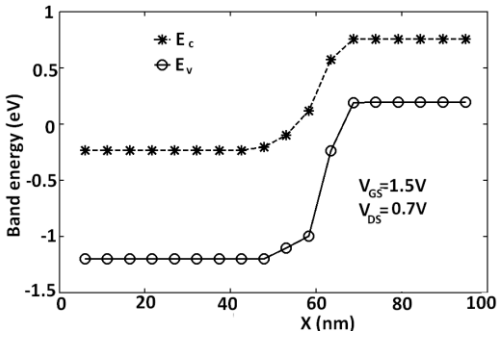


Figure 2: Energy band diagram at on condition. Tunneling takes place when gate voltage is applied. Drain channel junction is at 35 nm and source channel junction is at 65 nm. This energy band diagram is plotted at y=2 nm.

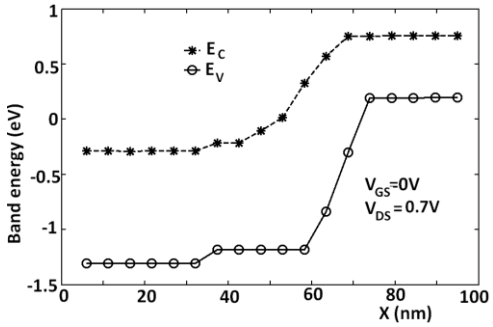


Figure 3: Energy band diagram at off condition, at y=2 nm. At this condition no tunneling takes place and hence the tunneling current is zero.

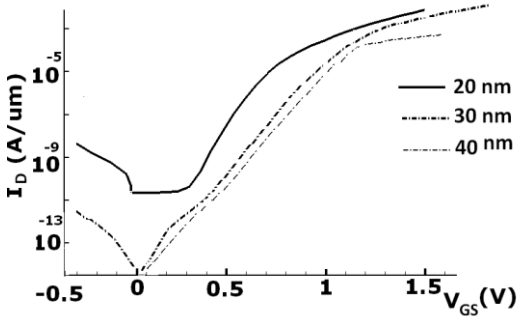


Figure 4: log I_D vs. V_{GS} curve is plotted for proposed device at various gate lengths. At 20 nm high on current is achieved.

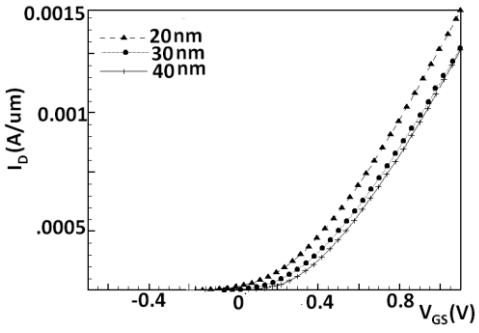


Figure 5: Linear I_D vs. V_{GS} curve is plotted for proposed device

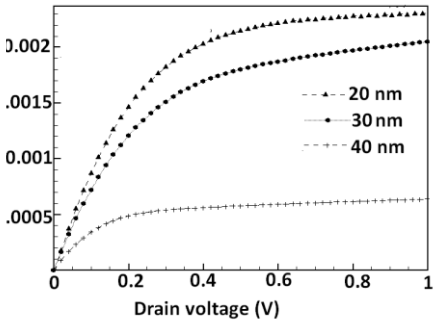
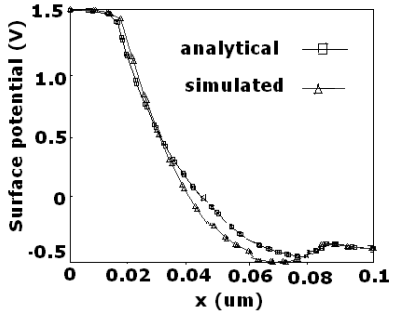


Figure 6: I_D - V_{DS} curve proposed device.



gure 7: Surface potential for the proposed device at 20 nm gate length.

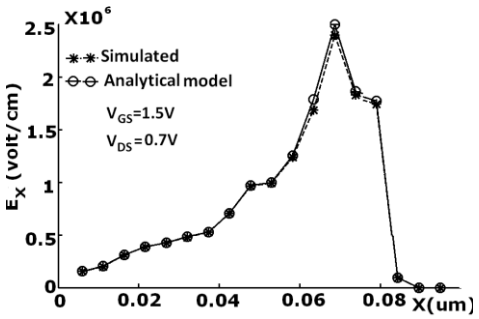


Figure 8: Variation of horizontal component of Electric field (Ex) along channel, y=5 nm. The local high electric field occurs at tunneling junction when gate voltage increases.

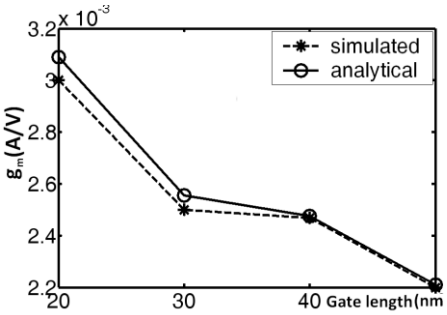


Figure 12: Analytical and simulated transconductance. Transconductance increases with the scaled gate length.

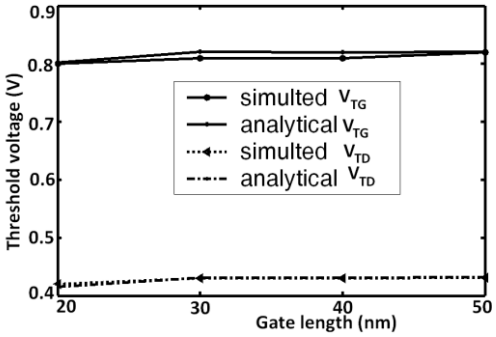


Figure 16: Comparison of simulated and analytical model. The drain threshold voltage is almost half that of gate and hence energybandgap is a strong function of V_{DS} is well agreed.

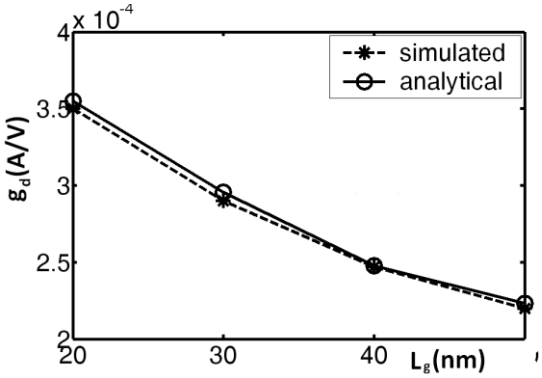


Figure 13: Analytical and simulated output conductance at different gate lengths.

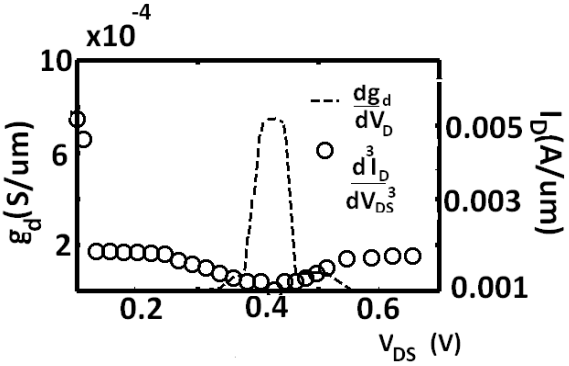


Figure 15: V_{TD}= 0.42 volts, V_{GS} =1.5 V as seen from the graph, 20 nm gate length.

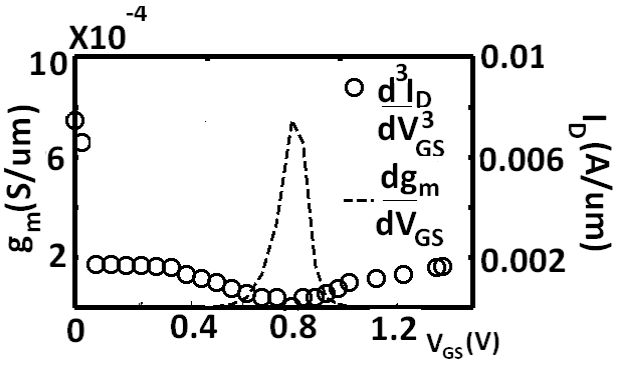


Figure 14: VTG = 0.8 volts, VDS=0.7 volt, 20 nm gate length.

5. CONCLUSION

A hetero gate dielectric double gate tunnel FET with low band gap source material has 53mV/dec subthreshold swing, on current in the range of mA, and better immunity to short channel effects. Analytical models for electric fields, drain current, sub threshold swing, transconductance, output conductance, gate and drain threshold voltages are also derived. The model results found to agree well with the 2D simulated results. Thus, the approximations used to arrive at manageable analytical expressions are quite acceptable.

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