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Current Mode Controller Analysis for Enhancing Quality of Power in Distribution System

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ABSTRACT
In this paper, new control strategy based on current mode control for Dynamic Voltage Restorer (DVR) is proposed to mitigate the power quality problems in the supply voltage. The simulated DVR is controlled indirectly by controlling the supply current. The reference supply currents are estimated using the sensed load terminal voltage and the DC bus voltage of DVR. The control scheme is based on synchronous reference frame theory(SRFT) for the operation of capacitor supported DVR. The contol strategy is verified through the extensive simulation studies using MATLAB with its simulink and Power Systems Block set (PSB) toolboxes to demonstrate the improved performance of DVR

Keyword
DVR, custom power device, current control, PSB, SRFT, Power Quality.

1. INTRODUCTION
Power quality problems in the distribution systems are addressed in the literature [1-3] due to the increased use of sensitive and critical equipments in the system. Some examples are equipments of communication system, process industries, precise manufacturing processes etc.
Power quality problems such as transients, sags, swells and other distortions to the sinusoidal waveform of the supply voltage affect the performance of these equipments. The technologies like custom power devices are emerged to provide protection against power quality problems. Custom power devices are mainly of three categories such as series-connected compensator like dynamic voltage restorer (DVR), shunt connected compensator such as distribution static compensator (DSTATCOM), and a combination of series and shunt- connected compensators known as unified power quality conditioner (UPQC) [2, 4-6]. The series connected compensator can regulate the load voltage from the power quality problems such as sag, swell etc. in the supply voltage. Hence it can protect the critical consumer loads from tripping and consequent loss of production [2]. The custom power devices are developed and installed at the consumer point to meet the power quality standards such as IEEE-519 [7]

A DVR is used to compensate the supply voltage disturbances such as sag and swell. The DVR is connected between the supply and sensitive loads, so that it can inject a voltage of required magnitude and frequency in the distribution feeder. The DVR is operated such that the load voltage magnitude is regulated to a constant magnitude, while the average real power absorbed/ supplied by it is zero in the steady state. The capacitor supported DVR is widely addressed in the literature [8-13]. The instantaneous reactive power theory (IRPT) [6],
sliding mode controller [9], instantaneous symmetrical components [2,13] etc., are discussed in the literature for the control of DVR. In this paper a new control algorithm is proposed based on the current mode control and proportional-integral (PI) controllers for the control of DVR. The extensive simulation is performed to demonstrate its capability, using the MATLAB with its Simulink and Power System Blockset (PSB) toolboxes.

2. PRINCIPLE OF OPERATION OF DVR
The single line diagram of a system with the DVR connected in series with the supply is shown in Fig. 1 (a). The DVR injects a voltage (Vc) in series with the terminal voltage at constant magnitude and the in-phase voltage (Vt) so that the load voltage (VL) is always constant in magnitude. Fig. 1(b) shows the phasor diagram of DVR when the terminal voltage is having sag (Vt) and swell (Vt ') in the voltage. The schematic diagram of a t three phase DVR connected to a three phase 3-wire system is shown in Fig. 2 (a). The source impedances (Za ,
Zb , Zc) are between the source and the terminal. The DVR uses three single-phase transformers (Tr) to inject voltages in series with the terminal voltage. A voltage source converter (VSC) along with a dc capacitor (Cdc) is used to realise a DVR. The inductor in series (Lr) and the parallel capacitor (Cr) with the VSC are used for reducing the ripple in the injected voltage. Fig. 2(b) shows the phasor diagram for the injected voltage and the fundamental voltage drop to maintain the dc bus voltage of DVR.VL 'and IL ' are the load voltage and current before the sag occurred in the supply system. After the sag event, the magnitude of the load voltage (VL), the load current (IL) and the power factor angle (Θ) are unchanged, but a phase jump is occurred from the pre-sag condition. The injected voltage (Vc) has two components. The voltage injected at quadrature (Vcq) with the current is to maintain the load is to maintain the load voltage at constant magnitude and the in-phase voltage (Vcd) is to maintain the dc bus of VSC and also to meet the power loss in the DVR. The control strategy of the DVR is to achieve these two components of the injection voltage and this is achieved by controlling the supply current. The currents are sensed and the two componentsof currents, one is the component to maintain the dc bus voltage of DVR and the second one is to maintain the load terminal voltages, are added with the sensed load current to estimate the reference supply current.

3. DVR CONTROL STRATEGY
The proposed algorithm is based on the estimation of reference supply currents. It is similar to the algorithm for the control of a shunt compensator like DSTATCOM for the terminal voltage regulation of linear and nonlinear loads [6]. The proposed control algorithm for the control of DVR is depicted in Fig. 3. The series compensator known as DVR is used to inject a

voltage in series with the terminal voltage.

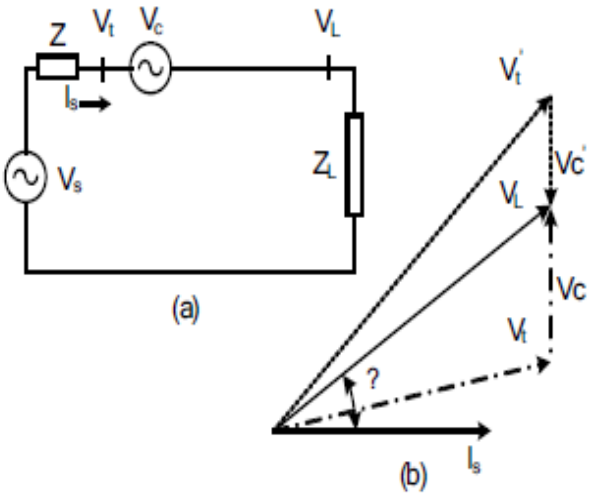

Fig. 1. (a) Single line diagram of DVR and (b) Phasor diagram

The sag and swell in terminal voltages are compensated by controlling the DVR and the proposed algorithm inherently provides a self-supporting dc bus for the DVR. Three-phase reference supply currents (isa *, isb*,isc *) are derived using the sensed load voltages (Vla, Vlb, Vlc), terminal voltages (Vta,Vtb, Vtc) and dc bus voltage (Vdc) of the DVR as feedback signals.

The synchronous reference frame theory based method is used to obtain the direct axis (id) and quadrature axis (iq) components of the load current. The load currents in the three-phases are converted into the d-q-0 frame using the Park's transformation as,

$$\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\theta & -\sin\theta & \frac{1}{2} \\ \cos\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta - \frac{2\pi}{3}\right) & \frac{1}{2} \\ \cos\left(\theta + \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) & \frac{1}{2} \end{bmatrix} \begin{bmatrix} i_{la} \\ i_{lb} \\ i_{lc} \end{bmatrix} \quad (1)$$

A three-phase PLL (phase locked loop) is used to synchronize these signals with the terminal voltages (Vta,Vtb, Vtc). The d-q components are then passed through low pass filters to extract the dc components id and iq. The error between the reference dc capacitor voltage and the sensed dc bus voltage of DVR is given to a PI (proportional-integral) controller of which output is considered as the loss component of current and is added to the dc component of id. Similarly, a second PI controller is used to regulate the amplitude of the load voltage (Vt). The amplitude of the load terminal voltage is employed over the reference amplitude and the output of PI controller added with the dc component of iq . The q resultant currents are again converted into the reference supply currents using the reverse Park's transformation. Reference supply currents (isa *, isb*,isc *) and the sensed supply currents (isa , isb, isc)are used in PWM current controller to generate gating pulses for the switches. The PWM controller operates at a frequency of 10 kHz and the gating signals are given to the three-leg VSC for the control of supply currents.

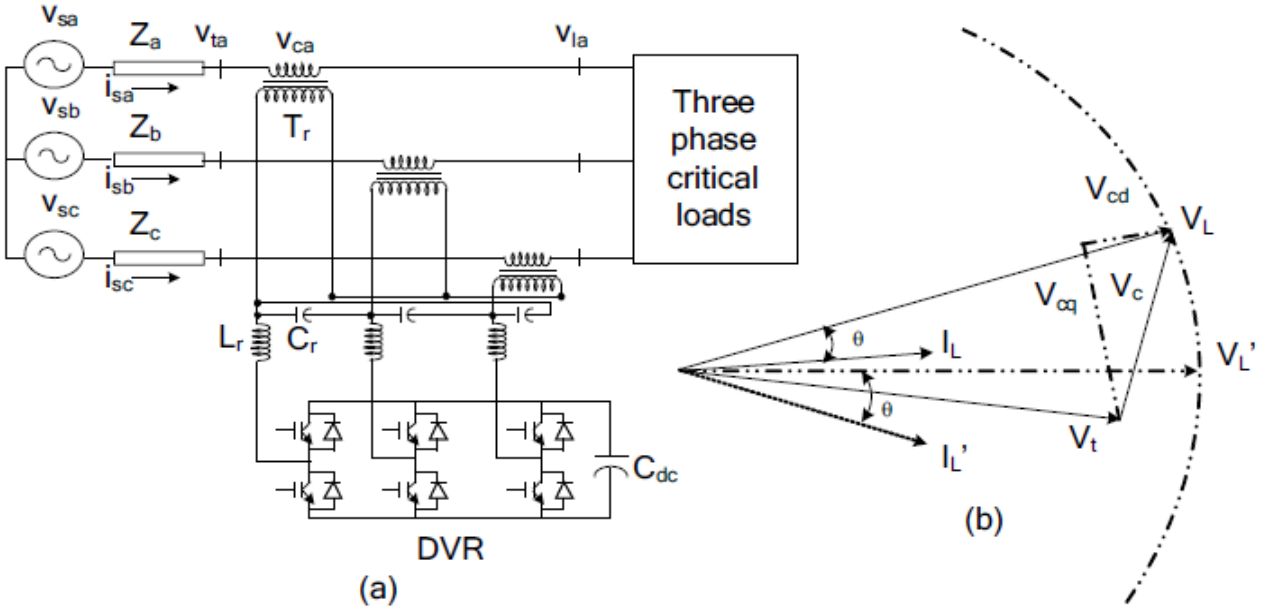

Fig. 2(a) Three phase DVR scheme and (b) Phasor diagram

4. MODELLING AND SIMULATION

The DVR is modeled and simulated using the MATLAB and its Simulink and Power System Blockset (PSB) toolboxes. The MATLAB model of the DVR connected system is shown in Fig. 4. The three-phase source is connected to the three-

phase load through series impedance and the DVR. The considered load is a lagging power factor load. The VSC of the DVR is connected to the system using an injection transformer. In addition, a ripple filter for filtering the switching ripple in the terminal voltage is connected across the terminals of the secondary of the transformer. The dc bus capacitor of DVR is selected based on the transient energy requirement and the dc bus voltage is selected based on the injection voltage level. The dc capacitor decides the ripple content in the dc voltage. The system data are given in Appendix. The proposed control algorithm is modeled in MATLAB as shown in Fig. 5. The reference supply currents are derived from the sensed load voltages, supply currents and dc bus voltage of DVR.

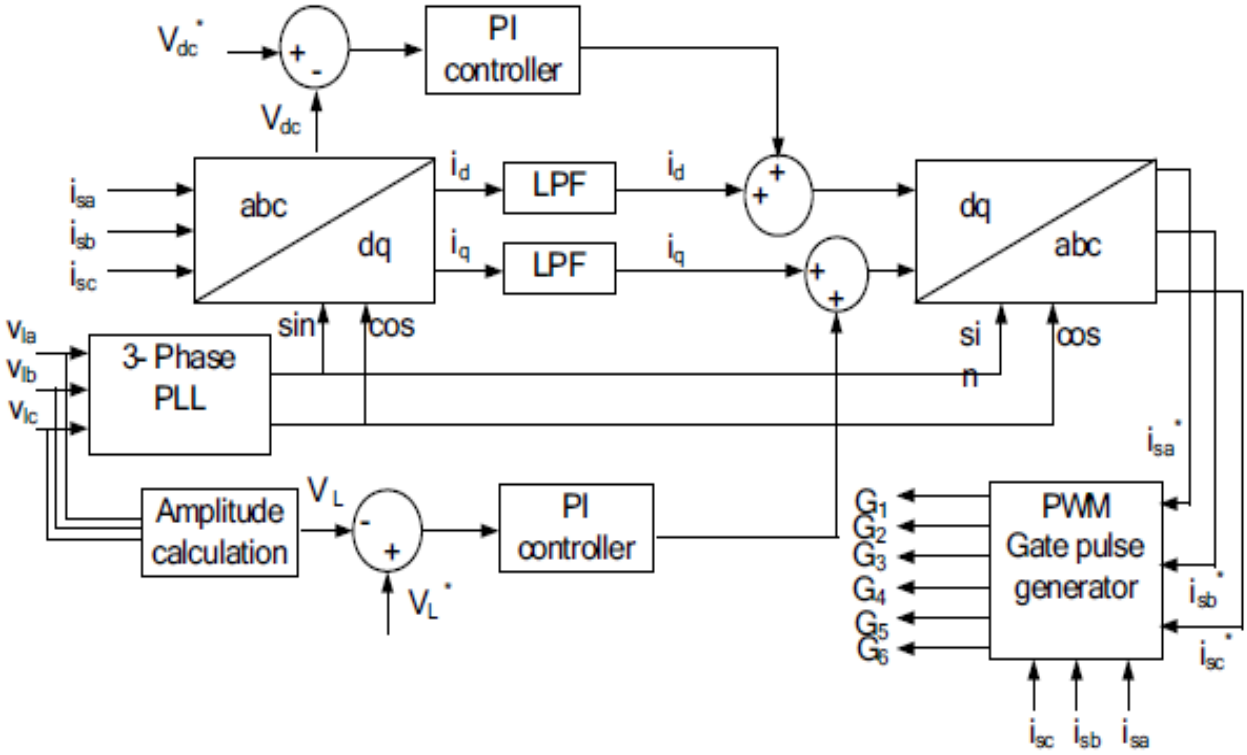

Fig. 3 Control Scheme of DVR

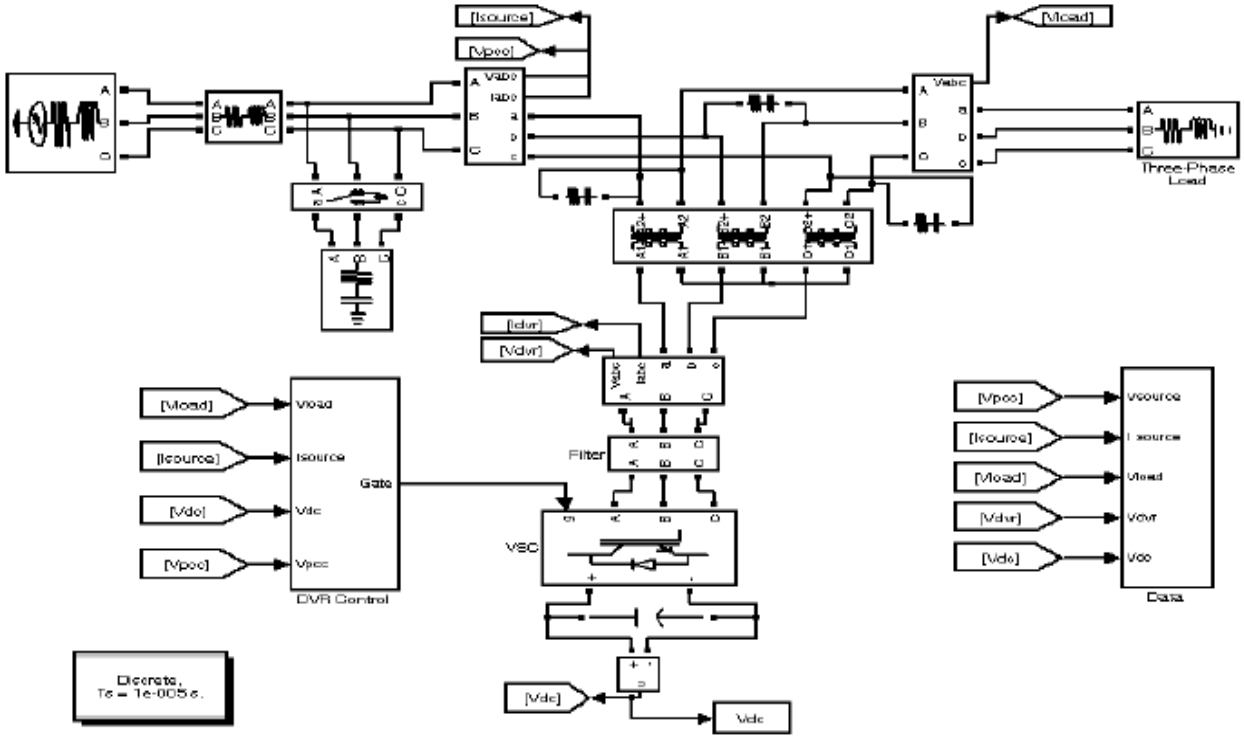

Fig. 4 MATLAB based model of three phase DVR connected system

The output of the PI Controller used for the control of dc bus voltage of DVR is added with the direct axis component of current. Similarly, the output of the PI controller used for the control of the amplitude of the load voltage is added with the quadrature axis component of the supply current. A pulse width modulation (PWM) controller is used over the error between reference supply currents and sensed supply currents to generate gating signals for the IGBT's (insulated gate bipolar transistors) of the VSC of DVR

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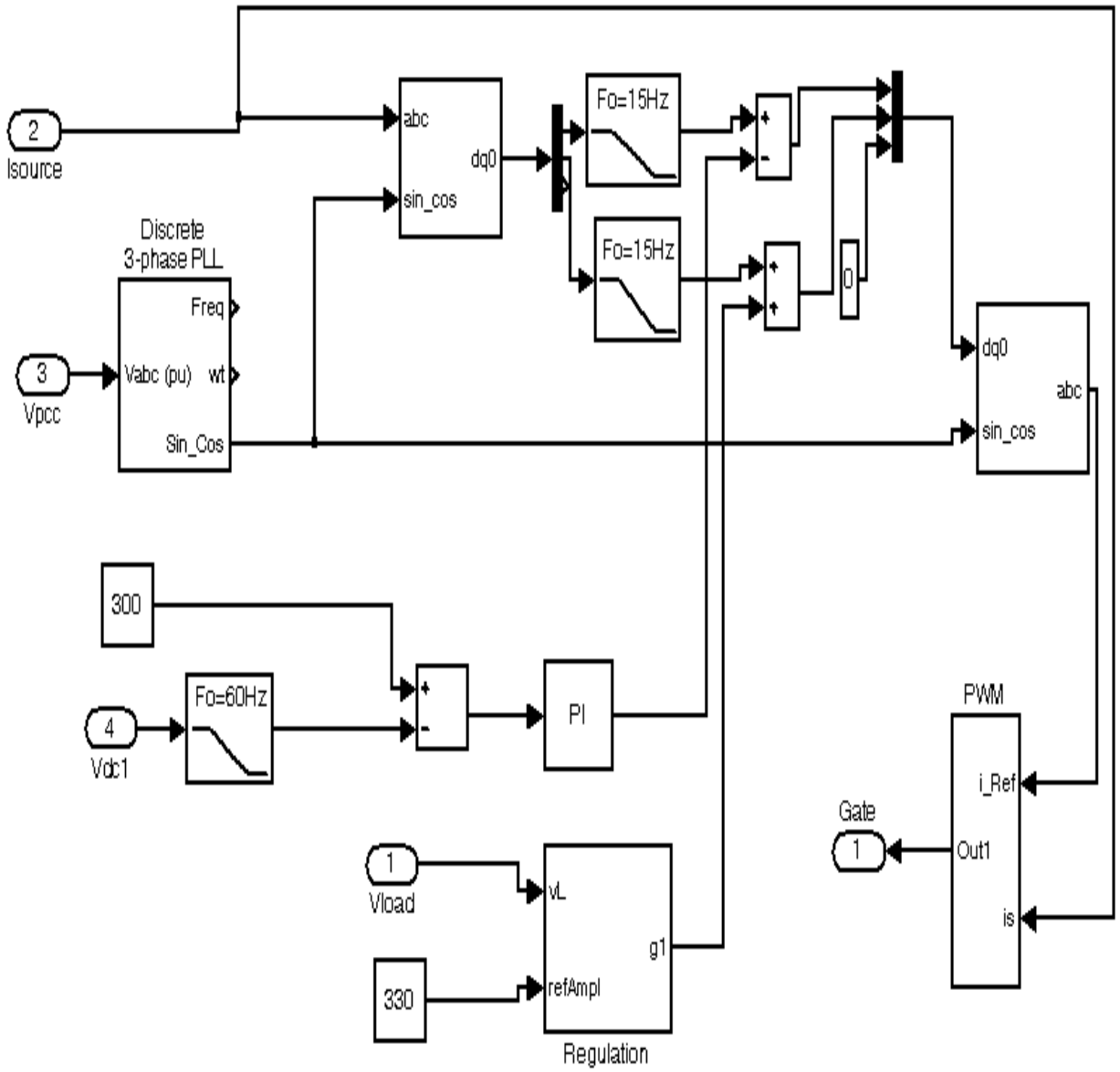

Fig.5. MATLAB based model of the proposed control method

5. RESULTS AND DISCUSSION

The proposed control scheme of DVR is verified through simulation using MATLAB software along with its Simulink and Power System Blockset (PSB) toolboxes. The DVR is tested under different operating conditions like sag (Fig. 6) and swell (Fig. 7) at the terminal voltages (Vta,Vtb, Vtc).

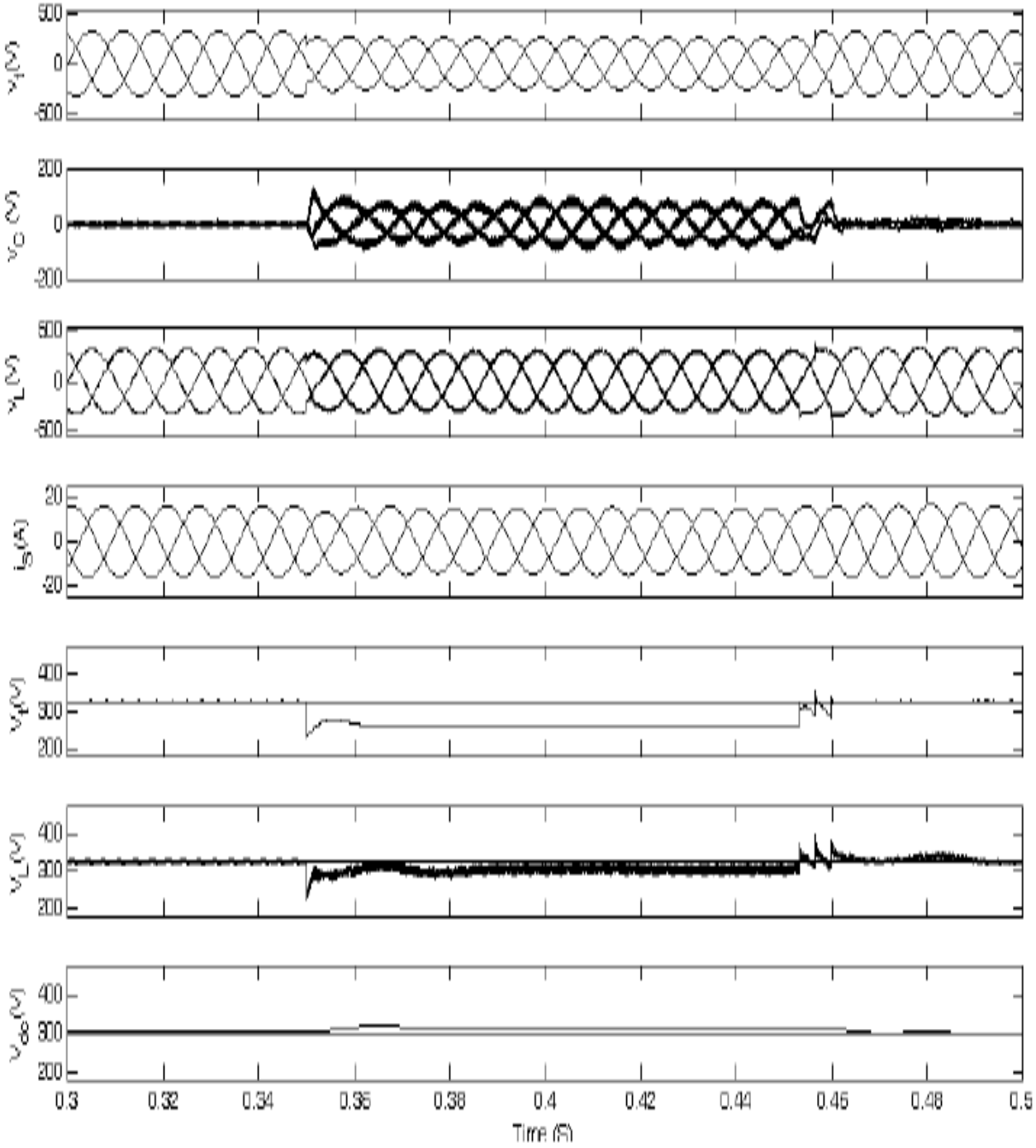

Fig.6 Dynamic behavior of DVR for voltage sag compensation

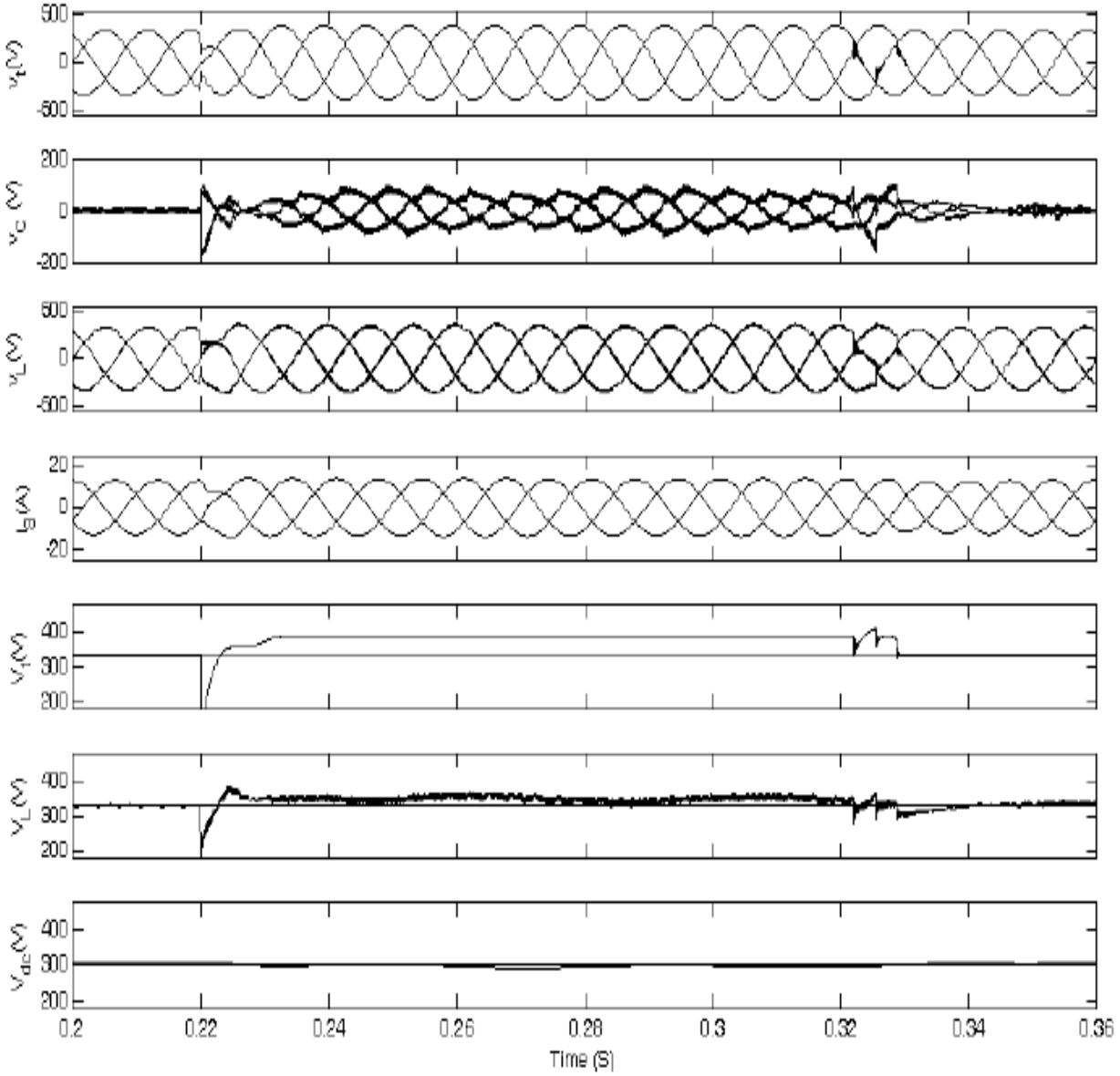

Fig.7 Dynamic behavior of DVR for voltage swells compensation

In Fig. 6, the terminal voltage has a sag of 30% with a magnitude at 70% of rated value at 0.26 sec and occurs up to 0.45 sec. The DVR injects fundamental voltage (Vc) in series with the terminal voltages (Vla Vlb Vlc). The load voltage is maintained at the rated value. The terminal voltage (Vt), supply current (is), amplitude of terminal voltage (Vt) the amplitude of load voltage (VL) and the dc bus voltage (Vdc) of DVR are also shown in the dc Fig. 6. It is observed that the dc bus voltage of DVR is maintained at reference value. Similarly, in Fig. 7, a swell in terminal voltage (Vt) has t occurred at 0.22 sec up to 0.32 sec and the load voltage (VL) is observed to be satisfactory due to the proper voltage injection by the DVR. The load voltage (VL) is maintained at the rated value. The terminal voltage (Vt) supply current (is), the amplitude of terminal voltage (Vt), the amplitude of the load voltage (VL) and the dc bus voltage (Vdc) of DVR are also shown in the Fig. 7. It is observed that the dc bus voltage of DVR is maintained at reference value, though perturbation is occurring during transients.

6. CONCLUSION

A new control strategy based on current mode control for Dynamic Voltage Restorer (DVR) has been proposed to mitigate the power quality problems in the terminal voltages. The proposed control scheme of DVR has been validated the compensation of sag and swell in terminal voltages. The performance of the DVR has been found very good to mitigate the voltage power quality problems. Moreover, it has been found capable to provide self- supported dc bus of the DVR through power transfer from ac line at fundamental frequency.

APPENDIX

The parameters of the system considered are:

Line Impedance, Ls = 3.5 mH, Rs = 0.01 Ω
Load: 8.5 kVA, 0.707 pf lag.
Ripple filter: Cr = 1 µF, Lr =3.1 mH.
DC bus voltage: Vdc = 300 V
DC bus capacitance: Cdc = 1000 µF
AC line voltage: V_{LL}= 415 V, 50 Hz
PWM switching frequency: 10 kHz
Transformer: 4.8 kVA, 200/400V

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