International Journal of Applied Information Systems (IJAIS) – ISSN : 2249-0868
Foundation of Computer Science FCS, New York, USA
2nd National Conference on Innovative Paradigms in Engineering & Technology (NCIPET 2013) – www.ijais.org

Multiple Access System based on ARM and 1-Wire Technology

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ABSTRACT
This paper presents a multiple hardware applications based on ARM and 1-wire protocol. In this paper, the single is used for different purposes like authentication, eCash, electronic toll tax system, vending purpose. The application has several components such as 1-wire network of iButton, EEPROM memory, LCD display.

Keywords
ARM, iButton, 1-wire communication protocol, GSM module

1. INTRODUCTION
In a traditional 2-wire implementation, the microcontroller requires minimum two port pins for data and clock signaling to the two port slave device. 2-wire slave device also requires an additional VCC pin for device operation. 1-wire communication protocol is a simple serial signaling protocol combining data and power into single signaling.

In the identification domain, traditional technologies are used, such as the magnetic stripes, the bar codes which are applied on the surfaces, the RFID labels. With these technologies one another technology is added, which is based on 1-wire communication protocol.

The iButton technology belongs to category of identification by touch. Along with identification, iButton can be used for money transaction like credit cards which is also known as electronic cash (e-cash). It is also used for vending purpose.

2. SYSTEM OVERVIEW
To achieve the goal, the following additional technical arrangements are implemented in the system. Multiple devices are controlled and processed by ARM. iButton is used to access the selected mode of the system. EEPROM is used to store the information of iButton along with its serial number. iButton uses 1-wire interface to communicate with ARM processor through which it performs identification function and money transaction function-Fig.1

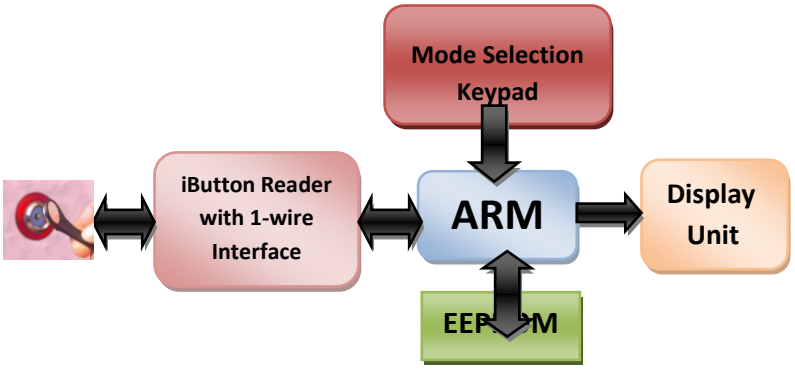

Figure 1. System Functional Diagram

3. IBUTTON AND 1-WIRE COMMUNICATION PROTOCOL
An iButton is a chip housed in a stainless steel enclosure. The steel iButton is rugged enough to withstand in harsh environments. It is small and portable enough to attach to a key fob, watch or other personal items. It can be used daily for applications such as access control to the building and computers, assets management and various data logging tasks.

It has the "lid" for 1-Wire data contact and the "base" for ground contact. Each contacts are connected to the silicon chip inside. The energy needed for operation is taken from the data line ("parasitic power"). The information within the iButton can be read by tapping it against a reader which consists of two metal probe contacts connected to the electronic reader circuit. The iButton system is more durable compared to swipe cards or other memory systems and it also has a larger memory capacity. Every iButton produced has a unique serial number and hence it will provide a very secure system. iButton is very hard to copy.

Every iButton has a laser-programmed ROM containing a 8-byte unique device ID, which includes 1-byte Cyclic Redundancy Check (CRC) verification field, 6-byte serial number and 1-byte family code- Figure 2

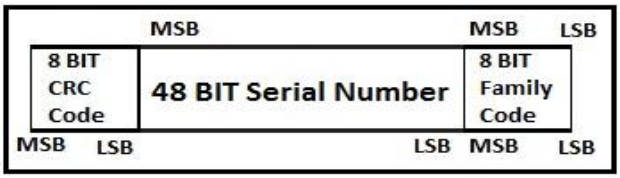

Figure 2. iButton 64- bit lasered ROM structure

The error detection method most effective at finding errors in a serial data sequence with a minimal amount of hardware requirement is the Cyclic Redundancy Check (CRC). The CRC can be most easily understood by considering the function as it would actually built in hardware, usually represented as arrangement of shift registers with feedback. The 1-Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 3. The polynomial is X8 + X5 + X4 + 1. Additional information about the 1-Wire Cyclic Redundancy Check (CRC) is available in Application Note 27: Understanding and Using Cyclic Redundancy Checks with Maxim iButton Products.

The shift register bits are initialized to 0 and then starting with the least significant bit of the family code, one bit at a time is shifted. After the 8th bit of the code has been inserted, the serial number is inserted. After the 48th bit of the serial number has been entered, the shift register finally contains the value of CRC. Shifting in the 8 bits of CRC returns the shift register to all 0s.

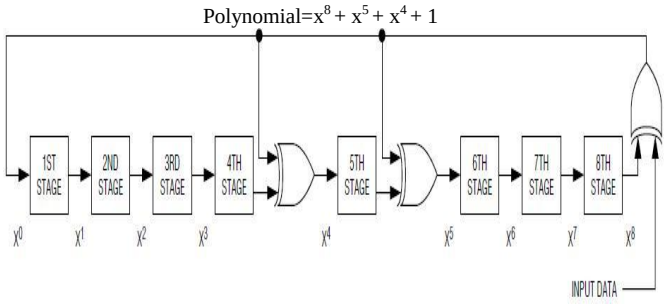

Figure 3. 1-wire CRC generator

1-wire communication protocol is a three phase transaction, it begins with reset line initiated by the master who brings all the devices on 1-line.The reset sequence is followed by device selection and function commands. Standard speed of 1-wire communication protocol is 15.4kbps.

A. The transfer of information between the host and the iButton uses the concept of time slot. Time slot is defined as the interval in which logic 1 or 0 is written or read over the 1-wire line. Master initiates the line by generating controlled low duration time pulse. Logic 1 is used to transmit a short low duration time pulse, while logic 0 is used to transmit a long low duration time pulse. The master or slave samples the line within the specified sample window to sense the logical level during the read or write sequence. The standard time slots ends at 60us. (Figure 3)

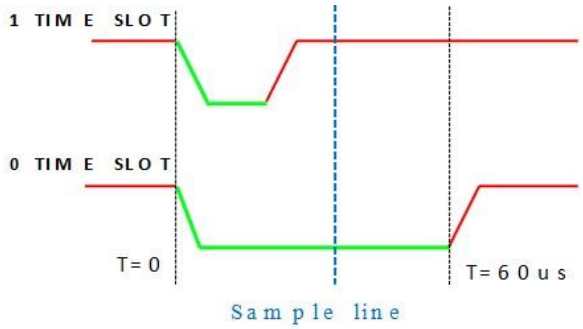

Figure 4. 1 time slot and 0 time slot

A.1. Master initiates the communication by issuing the reset pulse which s done by holding the 1 wire line low for more than 480us. After the bus master has release the line, it goes to the receive mode and waits for the period of 15us. During this time the 1-wire line returns to the logic high levels state of the supply voltage through an external pull-up resistor. After the 1-wire line return to the high state, all 1-wire slave devices on the bus acknowledge the master by pulling the line low for the period of 60us to 240us. This period is termed as "PRESENCE PULSE". By the end of 240us, the slave devises will have release the line and wait for returning the pulse to high state. At the end of recovery time slots, the 1-wire line ideals at high again. At this time, all the slave devices on 1-wire line are synchronized to a known state. In a multi-slave environment, all the devices will pull the line low simultaneously. Thus the master can determine the existence of slave device from the "PRESENCE PULSE" detection.

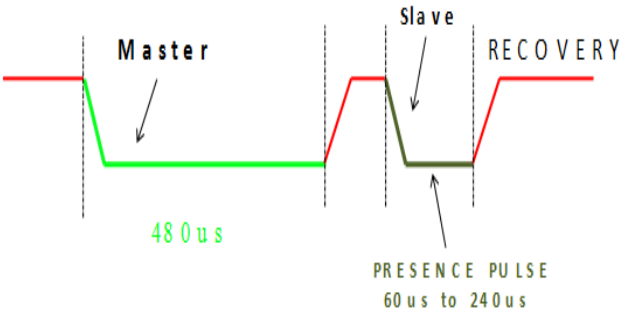

Figure 5. RESET and Presence Pulse waveform

A.2. Once the slave devices are synchronized to a known state, the bus master starts communicating with the slave devices. The master initiates the write-1 command by pulling low for definite duration and then it release the line. The 1-wire line is return back to a logic high state through an external pull up resistor. The 1-wire slave device starts its internal time base at the falling edge of the master and samples the line after a 15us. At this time, the bus master is ideal high state. The slave devices recognize the logic high bus status as a write-1 request.

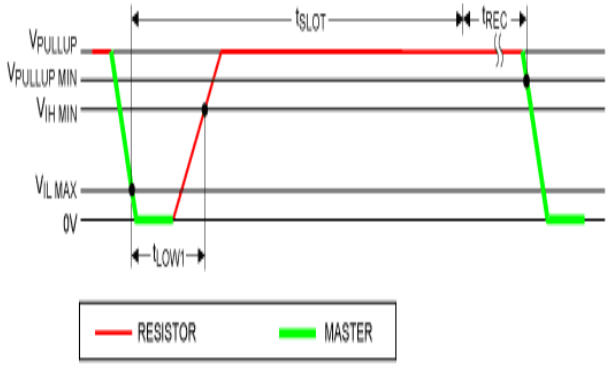

Figure 6. Write-1 time slot

A.3. The master initiates the write-0 command by pulling the low for minimum 60us and releases the line. The 1-wire slave device starts its internal time base at the falling edge of the master and samples the line at the maximum of 60us. Since the 1-wire line is active low, the slave device recognizes this state as a write-0 request.

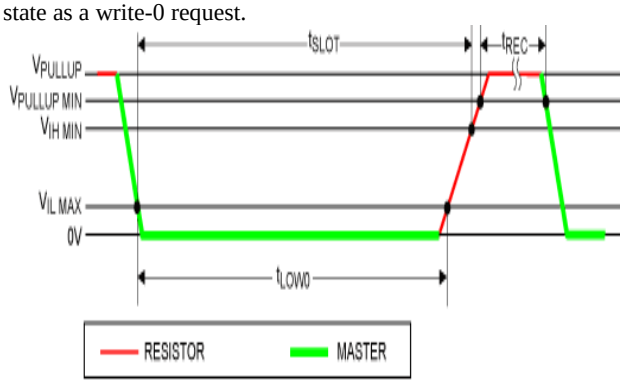

Figure 7. Write-0 time slot

The master initiates the slave read-1 command by pulling the line low and release the line.

A.4. The 1-wire line is return to a logic high state through an external pull-up resistor. The master samples the line at 15us (TMSR). At this time the 1-wire line is logic high state. The master recognizes the bus status as a read-1 (time slot)request.

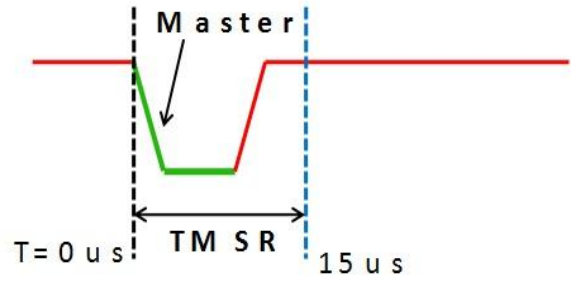

Figure 8. read-1 time slot

A.5. The master initiates the slave read-0 command by pulling the line low and it releases the line. The 1-wire line starts its internal time base at the falling edge of the master and pulls the line low for at least 15us. The master samples the line at 15us (TMSR) and recognizes the bus status as a read-0 request.

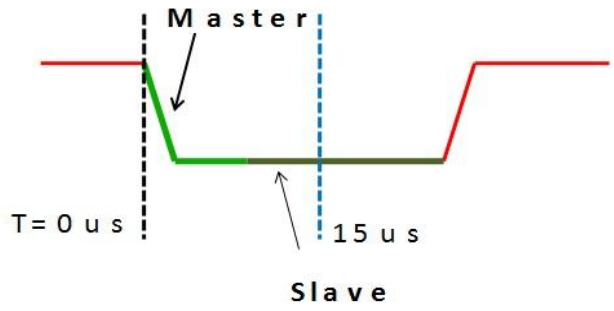

Figure 9. Read-0 time slot

The 1-wire command sequence has a three phases of transaction that begins with master generated reset sequence which is followed by the ROM command sequence in which host select its specific slave device based on its ROM ID then it perform specific device level function sequence such as write to memory or read from memory.

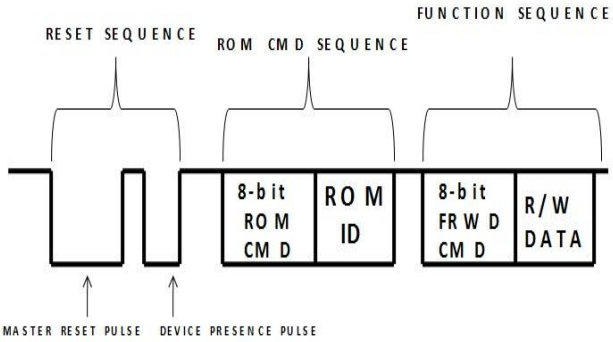

Figure 10. 1-wire command sequence

B. ROM FUNCTION COMMANDS

Once the bus master has detected a presence of the device, it can issue one out of four ROM function commands. All ROM function commands are eight bits long. A list of these commands follows (refer to flowchart in Figure11):

B.1. Read ROM [33h] or [0Fh]

This command allows the bus master to read the DS1990A's 1-byte family code, unique 6-byte serial number, and 1-byte CRC. This command can only be used if there is only a single DS1990A (iButton) on the bus. If there is more than one slave is present on the bus line, a data collision will occur when all slaves try to transmit at the same time. The DS1990A (iButton) Read ROM function will occur with a command byte of either 33h or 0Fh in order to ensure compatibility with the DS1990 (iButton), which will only respond to a 0Fh command word with its 8-byte ROM data.

B.2. Match ROM [55h] / Skip ROM [CCh]

The complete 1-Wire protocol for all Dallas Semiconductor iButtons contains a Match ROM and a Skip ROM command. Since the DS1990A (iButton) contains only the 8-byte ROM with no additional data fields, the Match ROM and Skip ROM are not applicable which will cause no further activity on the 1-Wire bus if executed. The DS1990A (iButton) does not interfere with other 1-Wire parts on a multidrop bus that do respond to a Match ROM or Skip ROM.

B.3. Search ROM [F0h]

When a system is initially starts, the bus master might not know the number of devices on the 1-Wire bus or their 8-byte ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 8-byte ROM codes of all slave devices on the bus. The ROM search process is the continuous repetition of a simple 3-steps: read a bit, read the complement of the bit, then write the desired value of the bit which is in the complementary form. The bus master performs this simple 3-steps on each bit of the ROM. After one complete pass process, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional pass processes.

B.4. Resume ROM

Resume command is used to restart the communication with selected device.

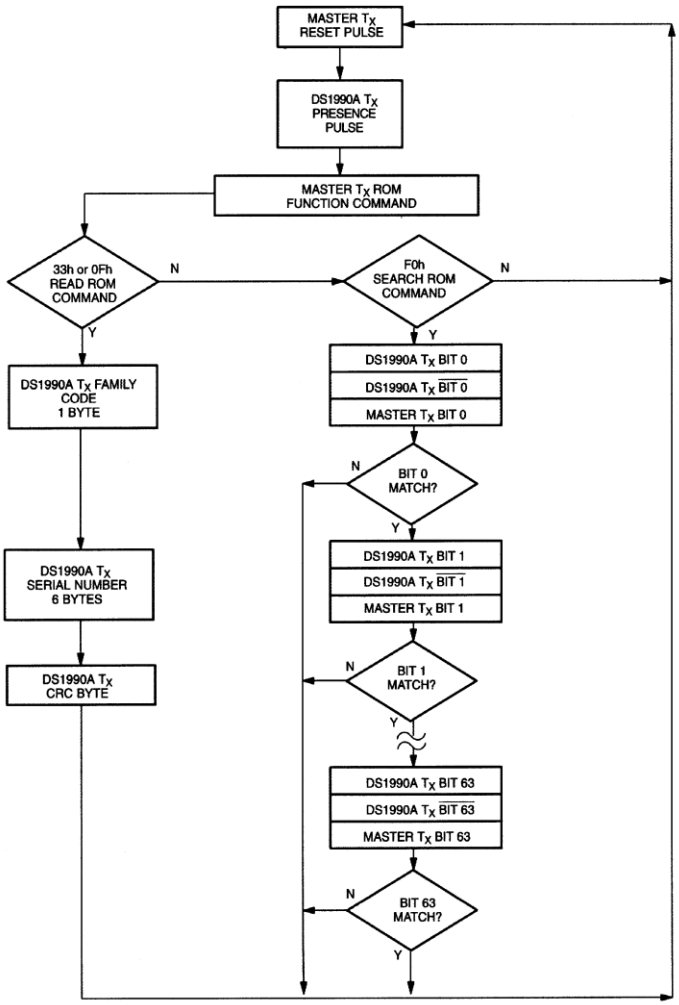

Figure 11. Flow chart of ROM function commands

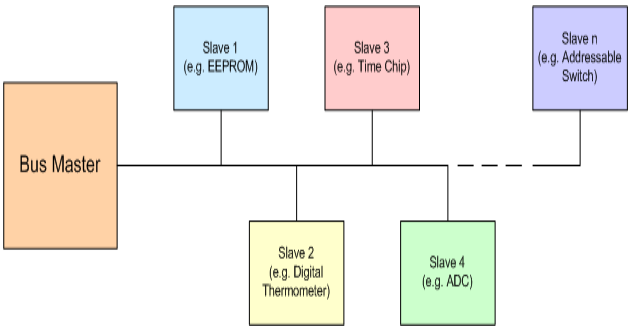

Figure 12. Connection of bus master with different slaves over 1-wire bus.

4. HEART OF THE SYSTEM 32bit MICROCONTROLLER ARM7

LPC2148 microcontroller is based on a 32bit

ARM7TDMI-S CPU that combines the microcontroller with embedded high-speed flash memory ranging from 32 kB. ARM or Advanced RISC Machine, uses a 32-bit RISC (Reduced Instruction Set Computer) processor which offers high performance and very low power consumption.

C. LPC2148 microcontroller is having following features:

C.1. The most important feature of ARM is its operating voltage is '3V to 3.6V'.

C.2. LPC2148 supports two UARTs and two fast I2C bus (400kbit/s) which is bidirectional, for inter-IC control uses only two wires: a Serial Clock Line (SCL), and a Serial Data line (SDA).

C.3. LPC2148 has a Real Time Clock in itself that uses a 3V reserved battery. Unlike other microprocessors, there is no need for an extra RTC IC.

C.3. LPC2148 provides two ADCs that has 2 analogy signal input from ADC0 and ADC1. ADC0 has 6 channels and ADC1 has 8 channels. The output is a 10-bit digital signal. It also provides one 10bit DAC that has 1 10-bit digital input and 1 output analogy signal.

C.4. LPC2148 used ARM7TDMI-S as its core and two types of buses to increase the board's performance. The modules which are inside connected by the CPU high performance bus called Advance High-Performance Bus (AHB) and the peripheral are connected by VLSI Peripheral Bus (VPB). The data between the two buses are exchange at the AHB and VPB bus connection.

C.5. The ARM7TDMI-S processor also employs a unique architectural strategy which is known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or the applications where code density is an issue. The main idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM7 processor has two instruction sets:

• The standard 32-bit ARM set.

• A 16-bit Thumb set.

The used of Thumb instruction set can reduce the size of the control program up to 65% and increases the performance up to 160%.

C.6. LPC2148 has two types of memories such as 8 kB to 40 kB of on-chip static RAM and 32 kB to 512 kB of on-chip flash memory.

C.7. The LPC2148 is equipped with a USB device controller that enables12 Mbps data exchange with a USB host controller.

C.8. 21 external interrupt pins are available in LPC2148.

DS1990 (iButton), 1-wire bus adopted unique master-slave, bit synchronization and semi-duplex serial data transfer to communicate with ARM. The type of the pull-up resistor was decided by the number of devices and the recovery time. Generally the pull-up resistor was between 0.6 to 5KΩ.

ARM required only 1 port pin for its connection with iButton probe to which iButton DS1990 is connected shown in figure 13.

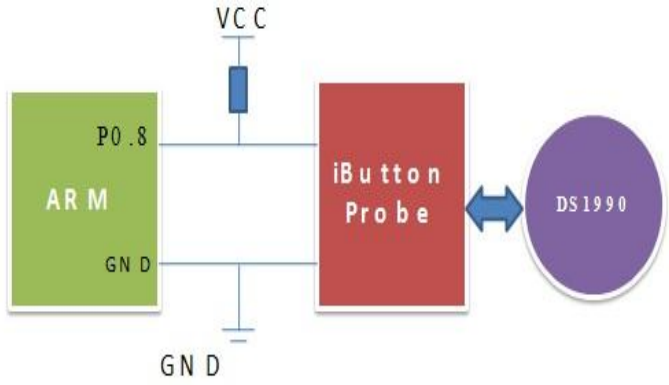

Figure 13. Interfacing between ARM iButton and ARM

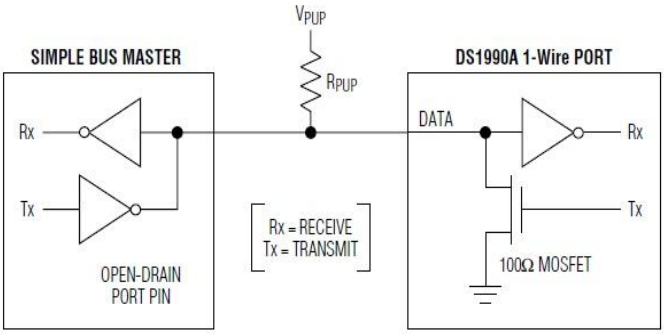

Figure 14. Equivalent circuit of ARM and DS1990A

5. HARDWARE STRUCTURE OF THE SYSTEM

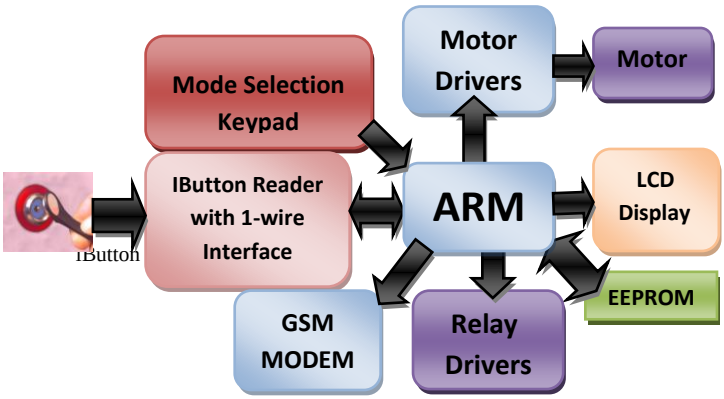

Figure 15. Hardware structure of the system

In the hardware structure, the heart of the system is ARM processor, along with the system consist of 1-wire communication device 'iButton ' with reader, external memory EEROM, motor drivers, relay drivers, GSM modem, keypad for mode selection and display unit.(figure 15)

LPC2148 microcontroller is used which is of 32bit and its operating voltage is 3V.The information within the iButton can be read by an iButton reader which consists of two metal probe contacts connected to the electronic reader circuit. Whenever iButton get access to the system, then it is used for authentication purpose. For that relay drivers are used which will be responsible for opening or closing the door. Along with authentication, it is used for eCash (electronic cash) like credit cards for money transaction, petrol filling, e-toll tax and vending purpose. For permanent storage of iButton serial number, EEPROM is used. GSM modem is used for the notification purpose.

6. CONCLUSION

The iButton is definitely the most robust of the existing hardware token devices. Wide variety of the systems based on application of iButtons and 1-wire communication protocol have been developed and successfully implemented in various application areas. This paper proposes one more potentially very beneficial solution, where iButton electronic ID technology and 1-Wire communication protocol are employed for the multiple access such as user authentication, vending, fare collection, eCash applications such as money transaction like credit cards, swapping the card while shopping.

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