International Journal of Applied Information Systems (IJAIS) – ISSN : 2249-0868
Foundation of Computer Science FCS, New York, USA
2nd National Conference on Innovative Paradigms in Engineering & Technology (NCIPET 2013) – www.ijais.org

Comparative Study of Turbo, LDPC Encoder and Decoder

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ABSTRACT
To assemble heightening information rate for radio communication, existing way, technology turn pathetic, achieving tolerable usable spectrum budget looking at future trust. This survey paper present comparative study between well known encoder and decoder methods which are used for forward error correction. This paper discuss about LDPC, Turbo encoder decoder based on different architecture like , parallel architecture, throughput, efficiency, system hardware implementation, bit rate, block size, propagation delay, Complexity, BER, memory (FPGA) and logic gates (FPGA) required on FPGA. After studying we found turbo coding is mend than former for radio communication.

Keywords
Low Dencity Check bit Check, LDPC, Turbo, Convolution, Viterbi, Encoder, Decoder, Bit Error rate, Throughput.

1. INTRODUCTION
This paper present the comparative study of work on different encoder and decoder methods, considering bit rate, Complexity, BER, power consumption, memory (FPGA) and logic gates (FPGA). LDPC have superior FEC capability, and hence low-density check bit -check (LDPC) are widely used in space, radio communication.

This paper, multi-rate parallel turbo encoder, LDPC decoder architecture and study concerned to implementation on a Xilinx field programmable gate array (FPGA) device with Spartan-3 are discussed.

Lately, low-density check bit -check (LDPC) have pulled an of all time raising add up of tending because of best FEC capability. It has been convey that with the block length 107, it is possible to achieve 0.04 dB from the Shannon limit at a BER of 10-6[3];

As explained in Figure 1, a LDPC code is a linear block code depicted with a binary thin $M \times N$ matrix H. -check bit -check Each word of matrix H represent to a check bit and each column represents a extracted symbol. The count of extracted symbols N is the LDPC *code length*. The count of non-zero elements in a row (column) is determined as the row (column) weight dC (dV).

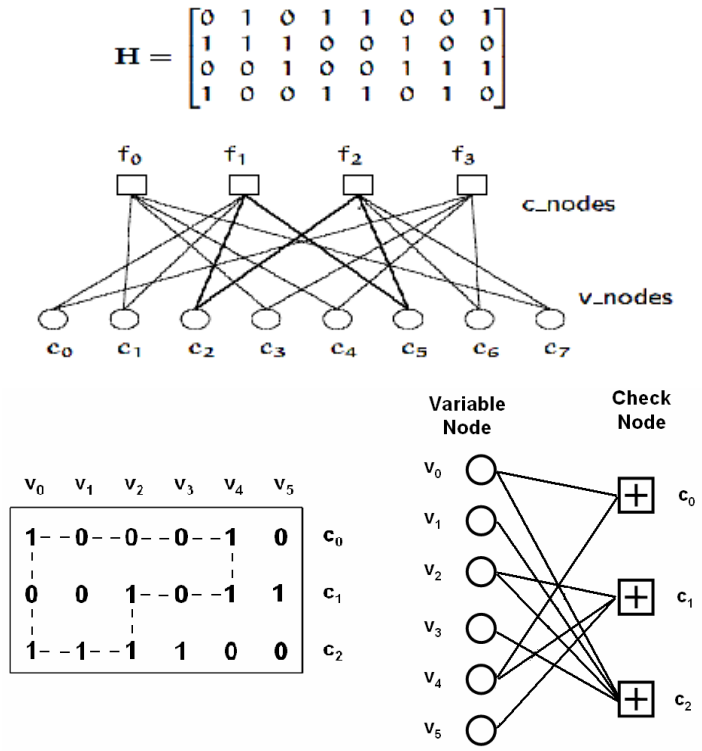

Figure 1. A irregular H matrix and its corresponding Tanner graph.

If all rows and all columns are of uniform weight, the LDPC code is called a *regular* code, otherwise an *irregular* code. The notion of Tanner graph has been introduced to represent LDPC codes.

Turbo codes were presented in 1993, by Berrou et al. [5] and since then these codes have received a lot of interest from the research community as they offer better carrying out than any of the other codes at very low signal to noise ratio. Turbo codes achieve near Shannon limit error correction carrying out with relatively simple component codes. A BER of is reported for a signal to noise ratio of 0.7 dB [5].

Efficient methodology for the application specific design reduces the time and effort spent during design space exploration. The turbo code application from the area of wireless communications is chosen as the key application for which an application specific design methodology is

developed. The functionality and specific characteristics of the application are needed to carry out the design space exploration. The application characteristics studied are, the affect on the carrying out of the turbo codes with variation in the size of the input message (frame-length), type of the interleaver and the count of decoding iterations. Turbo coding is a forward error correction (FEC) scheme. Iterative decoding is the key feature of turbo codes [5]. Turbo codes consist of chain of two convolution codes. Turbo codes give better carrying out at low SNRs (signal to noise ratio) [5].

Interestingly, the name Turbo was given to this codes because of the cyclical resubmit mechanism

(as in Turbo machines) to the decoders in an iterative way.

The turbo encoder carries the encoded bits which form inputs to the turbo decoder.

The turbo decoder decodes the data iteratively. Turbo codes can be chained in series, parallel or in a hybrid way.

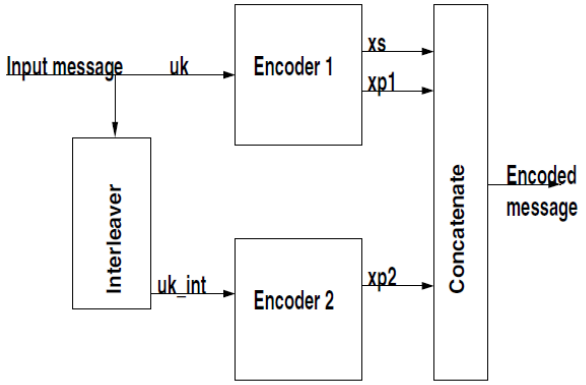

Fig2.(a) The encoder block schematic

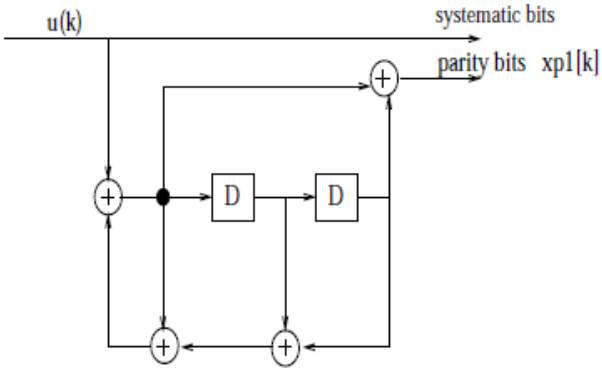

Fig2.(b) 4 state encoder details (Encoder 1 and

Encoder 2 are identical in nature)

The universal structure of a turbo encoder architecture consists of two Recursive Systematic

Convolutional (RSC) encoders Encoder 1 and Encoder 2. The constituent codes are RSCs because they combine the properties of non-systematic codes and systematic codes [6][4].

In the encoder architecture displayed in Figure 2 the two RSCs are identical. The *N* bit data block is first encoded by Encoder 1. The same data block is also interleaved and encoded by Encoder 2. The main purpose of the interleaves is to randomize burst error patterns so that it can be correctly decoded.

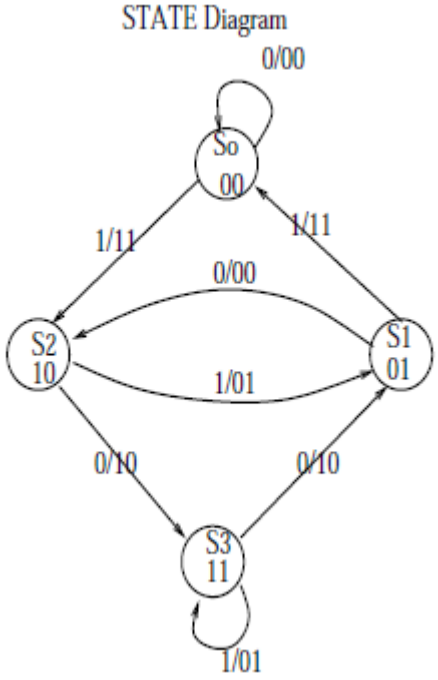

Fig2.(c) State diagram representation

The same data block is also interleaved and encoded by Encoder 2. The main purpose of the interleaves is to randomize burst error patterns so that it can be correctly decoded. It also helps to increase the minimum distance of the turbo code [5.57]. Input data blocks for a turbo encoder consist of the user data and possible extra data being appended to the user data before turbo encoding.

The encoder consists of a shift register and adders as shown in Fig. 2 (b). The structure of the RSC encoder is fixed for the design because enabling varying encoder structures would significantly increase the complexity of the decoder by requiring to adapt to the new trellis structure and computation of the different metrics in the individual decoders.

The input bits are fed into the left end of the register and for each new input bit two output bits are transmitted over the channel. These bits depend not only on the present input bit, but also on the two previous input bits, stored in the shift register.

2. LITRATURE SURVEY

Rosetta is the first is the first series of ESA deep space missions to be launched. The nominal return link margins of Rosetta at the comet encounter are 1.5dB below the requirement. It is therefore necessary to halve the return symbol rate from the scientist preferred rate. Moreover the link margins are also not met during other mission phases and other emergencies conditions. Similar condition are expected for mars express which is designed in strict commonality to Rosetta. Therefore NASA and ESA has investigated whether

Turbo code outperform the standard chained code by at least 1.5 dB on frame error rate[2].

Lei Yang [3] in his paper Code Construction and FPGA Implementation of a Low-Error-Floor Multi-Rate Low-Density Check bit -Check Code Decoder, With the superior error correction capability, low-density check bit -check (LDPC) codes have initiated wide scale interests in raidio communication, wireless communication, and storage fields. However, to cover a wide range of service requirements and diverse interference conditions in wireless applications, LDPC decoders that can operate at both high and low code rates are desirable. In this paper, a 9k code length multi-rate LDPC decoder architecture is presented and implemented on a Xilinx field programmable gate array (FPGA) device.

Rajeshwari M. Banakar [5] in his paper a lowpower design methodology for turbo encoder and decoder, the work is towards developing an application specific design methodology for low power solutions. The methodology starts from high level models which can be used for software solution and proceeds towards high carrying out hardware solutions. Turbo encoder/decoder, a key component of the emerging 3G mobile communication is used as our case study. The application carrying out measure, namely bit-error rate (BER) is used as a design constraint while optimizing for power and/or area.

Jason Kwok-San Lee [8] in his paper Memory-Efficient Decoding of LDPC Codes, present a low-complexity quantization scheme1 for the implementation of regular (3, 6) LDPC codes. The quantization parameters are optimized to maximize the mutual information between the source and the quantized messages. Using this non-uniform quantized belief propagation algorithm, they have simulated that an optimized 3-bit quantizes operates with 0.2dB implementation loss relative to a floating point decoder, and an optimized 4-bit quantizes operates less than 0.1dB quantization loss.

Yang Sun [1] in his paper high throughput, parallel, scalable ldpc encoder/decoder architecture for ofdm systems, presents a high throughput, parallel, scalable and irregular LDPC coding and decoding system hardware implementation that supports twelve combinations of block lengths 648, 1296, 1944 bits and code rates 1/2, 2/3, 3/4, 5/6 based on IEEE 802.11n standard. Based on architecture-aware LDPC codes an efficient joint LDPC coding and decoding hardware architecture.

Marjan Karkooti[9] in his paper Semi parallel architecture for real time LPDC coding, present error correcting codes enable the communication system to have a low power, reliable transmission over noisy channel. Low density check bit check codes are the best known ECC code that can achivedata rates very close to Shannon limit.In this present a semi parallel architecture for decoding low density check bit check codes.

Mohammad M. Mansour [7] in his paper High-Throughput LDPC Decoders, a high-throughput memory-efficient decoder architecture for low-density check bit -check (LDPC) codes is proposed based on a novel turbo decoding algorithm. The architecture benefits from various optimizations performed at three levels of abstraction in system design—namely LDPC code design, decoding algorithm, and decoder architecture.

Naoya Onizawa [10] in his paper 3.2-Gb/s 1024-b Rate-1/2 LDPC Decoder Chip Using a Flooding-Type Update-Schedule Algorithm, presents a high-speed low-density check bit check (LDPC) decoder chip using a new decoding algorithm, called a flooding-type update-schedule algorithm. Since node computations are performed using partially updated messages in the proposed algorithm, because of the good similarity among time-consecutive messages, data-transmission bottleneck between nodes for node computation is greatly reduced.

3. SYSTEM ARCHITECTURE

Above Figure 3 turbo code specification proposed for ccsds recommendation is summarized hereafter and depicted in figure 3.

3.1.Code type and rate

The code type rate is a systematic parallel chained turbo code with two component codes. The nominal code rate selectable with r =1/2, 1/3, 1/4, 1/6 bit per symbol.

3.2. Permuter

Permuter is fixed bit by bit permutation of the entire input frame of data

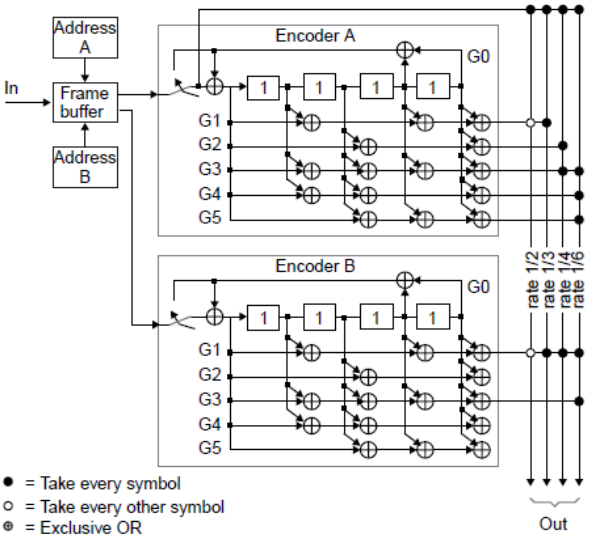

Figure 3: *Turbo encoder functional diagram*

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3.3.Code block specification

The resulting code block contain(k+4)/r encoded symbol,where r is nominal code rate. The additional 4 input bit are required for terminating the Trellis and actually implementing a block code.

3.4. Attached synchronization marker

The synchronized marker changed for the 4 code rate. The bit rate bits are relatedl to the code rate with the marker length being 32/r bit for r=1/2, 1/3,1/4 and 1/6.

3.5. Pseudo-randomizer The same interleaver can be used the turbo code, h(x)=x8+x7+x5+x3+1 The sequence

generator should be reset to the all one state at the start of each code block

4. ACKNOWLEDGMENTS

Turbo codes bring in 1993 have been widely heavily worked and explored by NASA, ESA and other space groups to examine feasibility to radio system. The exploration moves around on the CCSDS service and proposed code for espousal for CCSDS testimonial. Such good code which are with more complexity as even less complex , have achived gains ranging from 1.7 to 2.7dB depends on bit rate code and desired frame error rate. Pending final adoption at CCSDS level required, ESA is starting maturation of the required onboard chips and ground station equipment which are foreseen to be need for first time.

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