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Logic Gate Design using Ambipolar Carbon Nanotube Field Effect Transistors

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ABSTRACT

In this work, the performance of ambipolar carbon nanotube field effect transistor (CNTFET) is evaluated using Standford CNTFET model in a novel way. Carbon nanotube field effect transistor utilizing a semiconducting carbon nanotube (CNT) channel controlled by both polarity and regular gates. In this work, static logic gates and circuits based on ambipolar carbon nanotube field effect transistors (CNTFETs) using transmission – gate method have been designed. The power and delay performance of ambipolar carbon nanotube field effect transistor (CNTFET) has been investigated in basic logic gates and combinational logic circuits like half adder, full adder, half subtractor and full subtractor based on Standford Carbon nanotube field effect transistor (CNTFET) model.

Keywords

CNT, CNTFET, Transmission gate, Ambipolarlogic, Combinational circuits.

1. INTRODUCTION

Carbon nanotube field effect transistors (CNTFETs) have been proposed as an alternative to silicon CMOS technology [1]. Carbon nanotube field effect transistor logic devices offer high mobility for near ballistic transport, high carrier velocity for fast switching, as well as better electrostatic control due to the quasi one-dimensional structure of CNTs [2-5]. Carbon nanotube field effect transistors are of two types i.e. one is MOSFET type carbon nanotube field effect transistors (CNTFETs) and the other is schottkey –barrier type carbon nanotube field effect transistors (CNTFETs). Schttkey-barrier CNTFETs are ambipolar i.e. they conduct both electrons and holes, showing a superposition of p- and n- type behaviours. Ambipolar CNTFETs are having two types of gates namely polarity gate and the actual gate. The polarity gate controls the type of behavior i.e. n- or p- type and the actual gate controls the current flow through the transistor[6-7]. This new property of CNTFET produces a new logic circuits like a compact and in – filed reconfigurable universal 8- function logic gate [8-9] and in-field reconfigurable generalized NOR(GNOR) gates [10] to save circuit area.

In this work, the potential of ambipolar CNTFET has been exploiting the unique in-field controllability of the device polarity to design basic logic devices and circuits based up on SB-CNTFETs in a static transimission gate configuration. It has been shown that the output performance of CNTFET over Si-CMOS devices and are similar in the 45nm node experimental data. Unlike in the Si MOSFET, it is seen that the performance of a CNTFET is enhanced due to the novel feature i.e. ambipolarity.

2. AMBIPOLAR CNTFETS

Figure.1 shows a view and controllable characteristics of ambipolar CNTFETs. The top gate (control gate) in region A controls the current conduction through the transistor, while the back gate (polarity gate) in region B controls the type of polarity. A high or low voltage produces n- or p-type behavior. The working principle of ambipolar CNTFET is explained with the help of band diagram[3]. This transistor having a Schottkey barrier at the drain and source contacts that can be thinned by applying the right contact in region B. If the voltage applied at the electrode controlling the region B is positive and large enough (V+), then the Schottky barrier is transparent to tunneling electrons and the transistor has a n- type behavior. When the same voltage is negative and large enough (V_), then the Schottky barrier is transparent to tunneling holes and the transistor has a p- type behavior. The voltage in between these two values, the barrier is too thick for both electrons and holes and the conduction through the transistor is poor, and it is minimized for a PG bias $V_0=V_{ds}/2$ if V_{ds} is applied between drain and source. The conduction is also poor if the PG is left floating. While the choice of the voltage applied in region B determines the polarity of the devices, the voltage applied in region A may set up a high potential barrier in the middle of the channel and stop any potential current flow(Figure.2)

Generally the substrate can be used as a back gate operating as a PG means that all PGs are connected together. This reduces the opportunities for circuit design. To overcome this difficulty, another configuration is developed and is very compact device with top gating, which is shown in Figure.3

Ambipolar CNTFETs offer the opportunity of having in-field programmable ambipolar devices i.e. devices whose n- or p-type behavior can be programmed in field by using the polarity gate. This novel feature of ambipolar CNTFETs has been investigated in [10] where a compact and in-field reconfigurable logic gate that maps 8 different logic functions of 2 inputs by using only 7 CNTFETs has been presented.

3. LOGIC DESIGN WITH AMBIPOLAR CNTFETS

There are two types of logic designs i.e. one dynamic logic design and second one is static logic design. Dynamic logic design of ambipolar CNTFETs is compact and easy to use. However, it comes with all drawbacks of dynamic logic, namely signal racing and the difficult implementation of signal inversion, unless the circuit is made more complex. Static logic ambipolar CNTFET gates can therefore represent an attractive design option. Signal racing and signal inversion donot represent any challenge for static logic.

The basic transmission gate used for this design is shown in Figure.4. In this gate, both n- and p-type devices are in parallel. If one of the devices fails in passing the full signal, other devices necessarily restores the signal level.

4. RESULTS AND DISCUSSIONS

In this work, it has been simulated the right operation of logic gates with Standford CNTFET model for unipolar devices using lithography pitch of 45 nm.

Ambipolar behavior was modeled by fixing the polarity gate signals i.e. the device polarities during simulations, along the procedure suggested by I O Connor et al[4]. All results are in comparision to 45 nm technology node for CMOS.

In the simulations, logic gates have been simulated with equal rise and fall times, and the output current is equal to that of unit inverter. In CNT, electron mobility is equal to hole mobility, the on resistance of p and n-type CNTFET is equal. Thus, unlike CMOS gates, the PU devices in CNTFET gates need not be larger than the PD devices. This produces smaller CNTFET gates compared to the CMOS gates implementing the same function.

Inverter, NAND, NOR, AND, XOR, Half adder, Full Adder, Half substractor and Full substractor logic gates circuits have been implemented and two examples like Half and Full Adder are shown in Figures 5-6. The simulated result shows the excellent power, delay and PDP results (Table.1).

5. CONCLUSIONS

This paper describes the design of basic logic gates using CNTFET based on its unique property called ambipolarity. The basic logic gates and combinational logic circuits like half adder, full adder, half substrator and full substractor have been designed using ambipolar CNTFETs. The performance of these circuits are evaluated in terms power dissipation d=and delay factor and found that these circuits are superior performance when compared to normal logic circuits based on silicon and CNTFETs. In future, by using ambipolar CNTFETs, more complex circuits can be designed for communication and digital applications.

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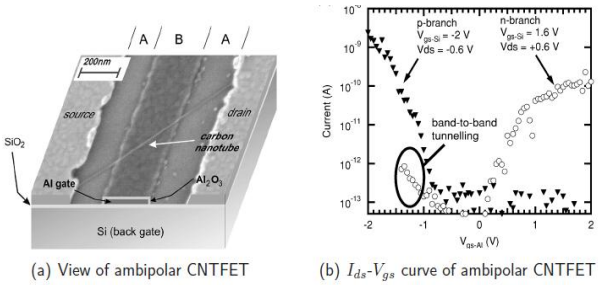


Figure.1: Ambipolar CNTFET view and characterization: (a) View based on a SEM of Ambipolar double-gate CNTFET. Region A is back gate and B is top gate. (b) I_{ds}-V_{gs} curve with top gate for a fixed back gate voltage. For a positive (negative) back voltage: device behaves as n- (p-) type.

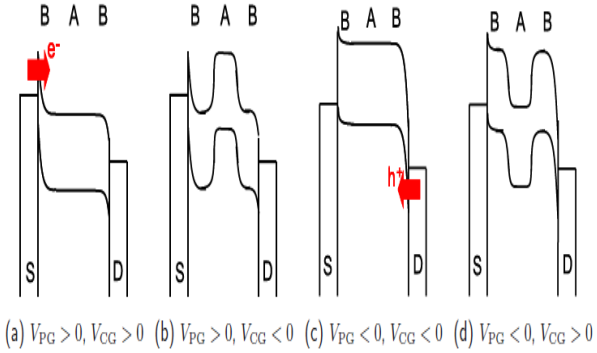
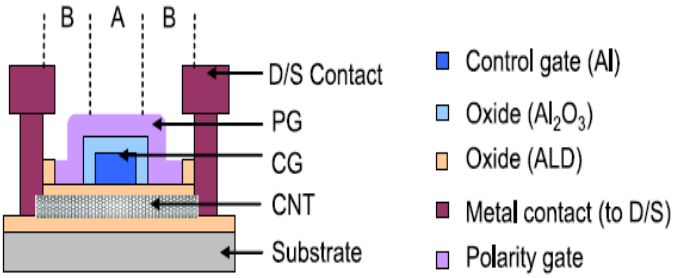


Figure.2. Band diagram of an Ambipolar CNTFET: (a) With V_{PG}>0 the CNTFET behaves as a n-type device. For V_{CG}>0, an electron current flows. (b) The n-type device blocks the electron current flow. (c) With V_{PG}<0 the CNTFET behaves as a p-type device. For V_{CG}<0, a hole current flows. (d) The p-type device blocks the hole current flow.



metallic CG is defined first by lithography. PG is defined on top and isolated by the native oxide of CG. Drain and source metal contacts are opened and passivated at the PG edges.

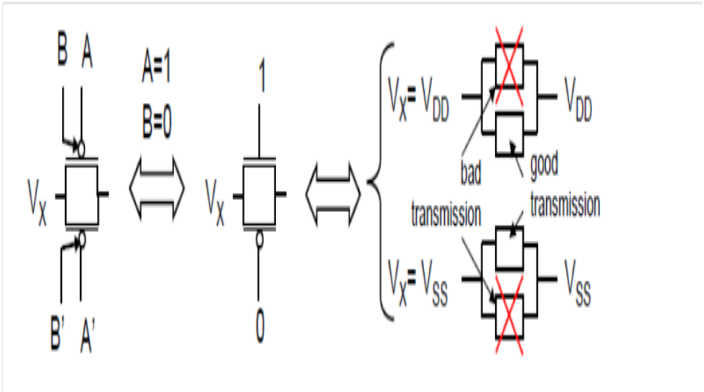


Figure.4: CNTFET Transmission gate: any passing configuration (A (+)B=1) prevents signal degradation.

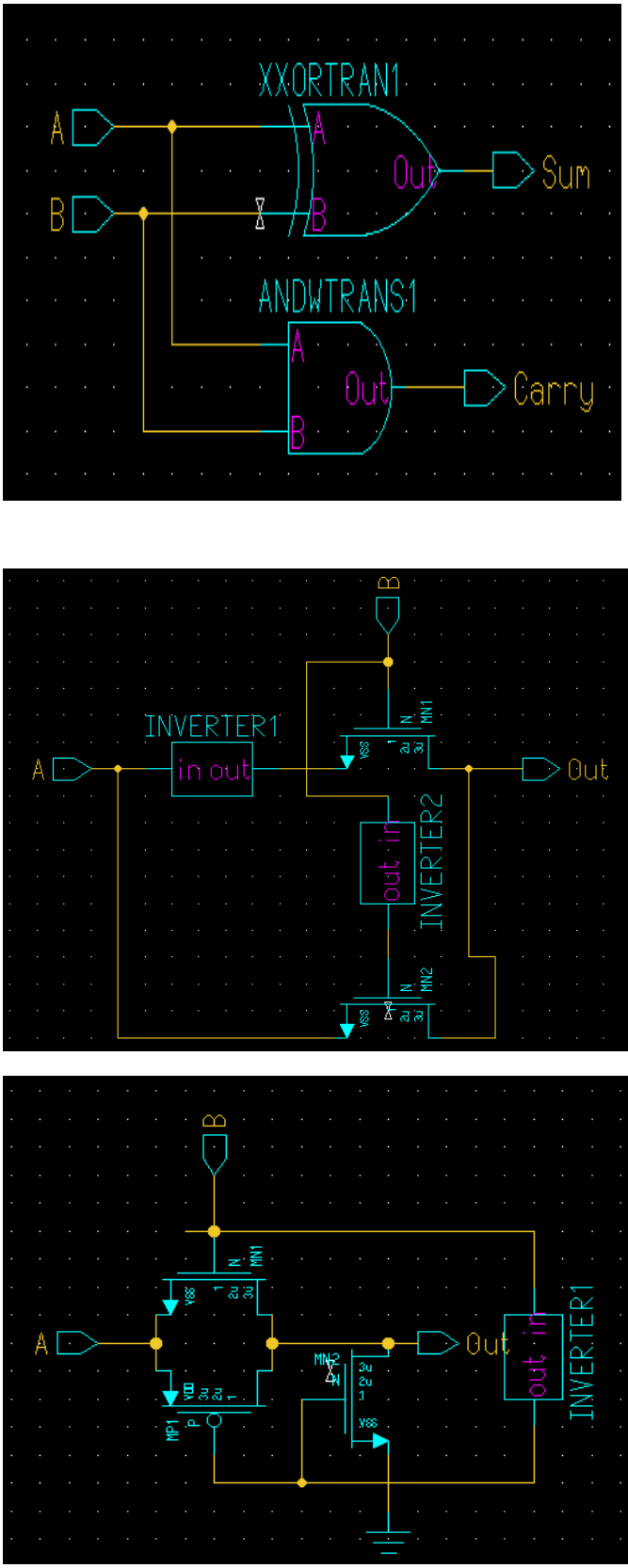


Figure.5: Half Adder implementation with Ambipolar CNTFET with transmission gates

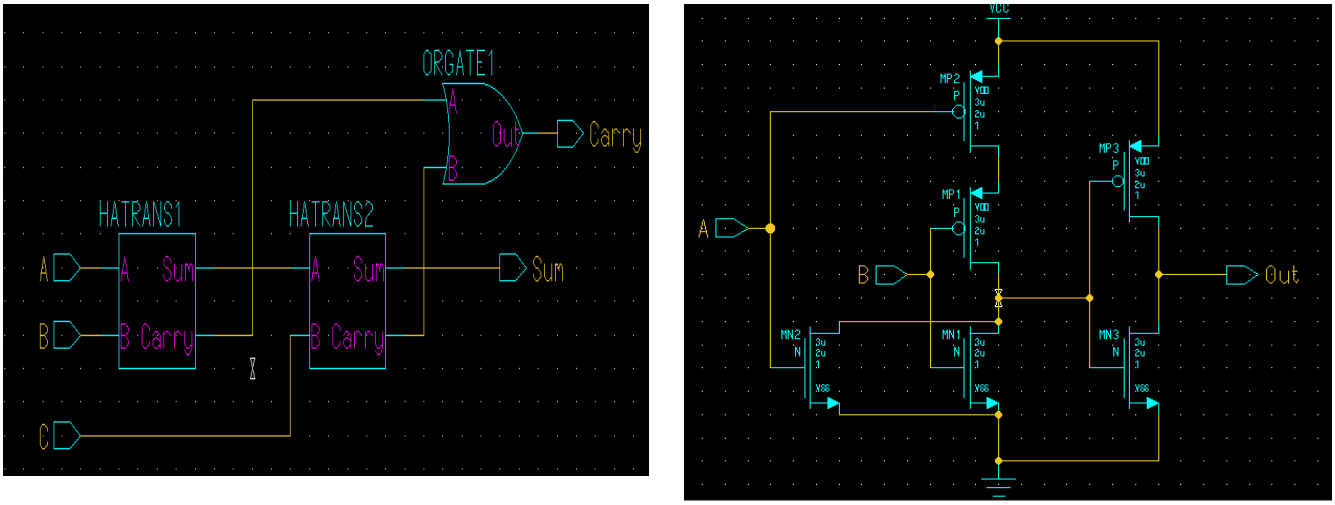
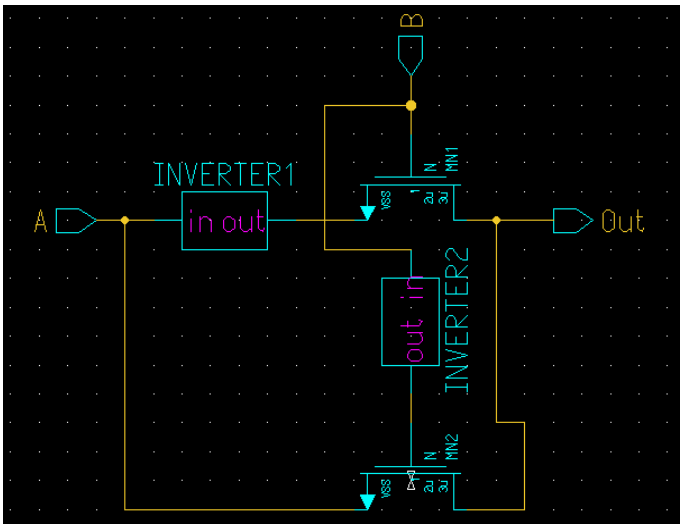


Figure.6: Full Adder implementation with Ambipolar CNTFET with transmission gates



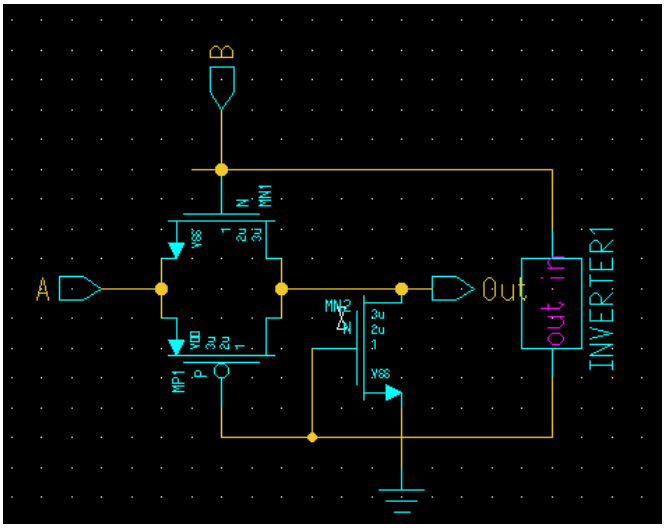


Table.1 Average Delay, Power and Power-Delay-Product(PDP) for Ambipolar CNTFET Based Design

Logic design	Ambipolar CNTFET design			Si CMOS design		
Logic Block	**Power (in Pw)**	**Delay**	**PDP (inx10^{-21}J)**	**Power**	**Delay**	**PDP**
Inverter	26.19	21.24ns	556.27	119.95 pW	40ns	4798x 10^{-21}J
NAND	14.50	24.28ns	38.78	15.4418 pW	48.883ns	754.84 x 10^{-21}J
NOR	60.01	21.42ns	1285.41	11.09 nW	40.15ns	445.26 x 10^{-18}J
AND	26.19	417.7ps	10941.3	31.7 pW	29.71ps	941.807x 10^{-24}J
OR	85.07	49.91ns	4246.35	11.11 nW	40.185ns	446.45 x 10^{-18}J
XOR	81.2	18.41ns	1494.89	4.47 nW	21.1ns	94.317 x 10^{-21}J
Half Adder	107.3	21.5ns	2306.95	4.5 nW	21.17ns	95.26x 10^{-21}J
Full Adder	299.8	10.73ns	3216.85	9.15 nW	66.13ps	605.08 x 10^{-21}J
Half Subtractor	186.9	21.7ns	4055.73	8.9 nW	21.20ns	188.6 x 10^{-21}J
Full Subtractor	458.3	943.9ps	432589	18.09 nW	319.83ps	5785 x 10^{-21}J