Basic Logic Gate design using Carbon Nanotube Field Effect Transistors

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ABSTRACT
In this paper, the performance of ambipolar carbon nanotube field effect transistor based logic devices have been evaluated using circuit compatible HSPICE model. The expression for drain current has been derived in terms of surface potential, specific voltage ξ_i(S/D), subband minima, source / drain Fermi levels and gate voltage. The PDP and EDP of basic carbon nanotube field effect transistor based logic devices have been investigated based on this HSPICE model.

Keywords
Carbon NanotubesCNT), HSPICE, Ambipolarity, CNTFET.

1. INTRODUCTION
Silicon-based technology has experienced phenomenal growth in the last few decades. A large part of the success of the MOS transistor is due to the fact that it can be scaled to increasingly smaller dimensions, which results in higher performance. Though this trend still continues, bulk MOSFET will soon reach its limiting size. For this reason, the semiconductor industry is looking for different materials and devices to integrate with the current silicon – based technology and in the long run, possibly replace it. The carbon nanotube field effect transistor is one among the most promising alternative due to its superior electrical properties. In general nanoscience the main research focuses on the search for new physical concepts and on creating the technology necessary for the development of nanodevices. But the usage of nanoscience for the engineering applications like communication circuits and memory devices is not achieved prominent position. In this research work, an attempt has been made to use nanodevices for electronic applications in digital logic.

Carbon nanotubes are sheets of graphite rolled in to the cylinders. Depending on the direction in which the nanotubes are rolled (chirality) they can be either metallic or semiconducting [1]. Since the discovery of carbon nanotubes in 1990, there has been great research concerning the electrical properties of carbon nanotubes [2-4]. The semiconducting nanotubes have been used in high performance transistors where the channel is the nanotube itself.

CNTFETs can be used to construct logic gates in two ways. First one is to replace MOSFET with CNTFET, creating present logic functions directly to a new technology. To improve the performance gain with CNTFET, first it is necessary to develop a compact model for CNTFET which helps not only logic designer, but also application engineer for the evaluation of new circuits with CNTFET. Second one is to use specific properties of CNTFET like ambipolarity, allowing the creation of completely new logic functions, inaccessible to MOSFET based circuits. In this work, the first one is explained in detailed manner.

There have been great research interest in analysing carbon nanotube based devices as it offer high mobility for near – ballistic transport, high carrier velocity for fast switching [5-7]. The carbon nanotube field effect transistor thus already achieved widespread attention as possible alternative nanoscale transistor. Now ambipolar Carbon nanotube field effect transistor is a new device and its I-V characteristics are similar to that of MOS devices, qualitatively most of the CMOS circuits can be implemented using ambipolar carbon nanotube field effect transistors. Therefore, there is a need for developing compact SPICE model for the ambipolar carbon nanotube devices. In this paper, the model for ambipolar carbon nanotube field effect transistor using H-SPICE has been explained. The SPICE compatible circuit model of ambipolar carbon nanotube field effect transistor is implemented in H-SPICE for the circuit simulations. This model is used to evaluate the performance of the logic gates as well as combinational logic circuits based on ambipolar carbon nanotube field effect transistors and the simulation result shows excellent performance on power and speed of operation.

The remainder of the paper is organised as follows. Section II describes the basic characterization of ambipolar carbon nanotube field effect transistors. Section III describes the model for ambipolar carbon nanotube field effect transistor which have used for this simulations. Section IV describes the logic circuit realization using ambipolar carbon nanotube field effect transistors and the results are compared with silicon devices. Finally, conclusions provided in section V.

2. Basic Characterization of Ambipolar CNTFET
An ambipolar CNTFET behaves either as p-type or n-type depending on gate bias conditions. This property motivates the use of the back gate as a second gate, which controls the n-or p-type polarity of the transistor. Such devices have two gates: one of them operates as a polarity gate (n- or p- type), while the other gate operates as a conventional gate (on and off state).

Several techniques to manufacture such in-field programmable CNTFET has been proposed in literature [8-9]. A sample cross section is shown in Figure.2(a), with the layout drawn in Figure.2(b). The gate G in region A turns the device on or off, as the regular gate of MOSFET does, polarity gate PG in region B controls the type of polarity setting to P- or n-type.

Based on simulation results, the characteristic curves are plotted for ambipolar CNTFET. For this simulation, it have considered the diameter of the nanotube as 13nm, the thickness of high K top gate dielectric material (planar gate) is 4.0nm and the dielectric constant of the high-K top gate dielectric material (planar gate) is k = 16. For plotting the characteristic curves, the drain current (I_d) have been taken for different gate voltages (V_g) and drain voltages (V_d). Transfer characteristics for different drain voltages are plotted in Figure 3(a), which shows that the drain current first decreases and then increases with increasing gate source voltage, exhibiting p-type behaviour with dominant hole conduction and n-type behaviour with dominant electron conduction respectively. The range of gate voltage considered is 0V to 0.9 V and plots are drawn for different drain voltages (V_d) 0.1V, 0.2V, 0.3V, 0.4V and 0.5V for fixed dielectric constant k=16.

The output characteristics curves ($I_d \sim V_d$ curves) also have been plotted for different applied gate voltages which are shown in Figure 3(b). The range of drain voltage considered is 0V to 0.9V and plots are for different gate voltages 0.2V, 0.25V and 0.3V. The drain current is almost zero for the gate voltage 0.2V for n-type CNTFET. The drain current increases with applied gate voltages.

3. Model for Ambipolar CNTFET

Before going in to the realization of digital circuits using CNTFETs, first the simulation model used in this paper is discussed. The compact model of MOSFET like CNTFET is presented, first developed by Purdue University [10] which is explained below. It is a surface potential – based SPICE compatible model which is used to simulate the CNT's with ballistic behaviour.

This model is applicable to a range of CNTFETs with diameter between 0.8 to 3 nm. Quasi-static characterization (I-V) have been modelled and validated with excellent harmony. The computational procedure to evaluate the drain current I_D and the total channel charge Q_{CNT} is shown in Figure.4. The main quantities used in the model are the control potential V_{CNT} and the specific voltage ξ_i(S/D) that depends on the control potential, the subband energy level ΔP and the source (drain) Fermi level $\mu_{S/D}$ and the specific voltage is given by

$$\xi_i = (V_{CNT} - \Delta P - \mu_{S/D}) / K_B T \quad (1)$$

Here K_B is the Boltzman constant, and T is the operating temperature. When the conduction band minima for the first subband is set to half the nanotube band gap Δ_1, with $\Delta_1 \approx 0.45/$ diam (in eV), then the pth equilibrium conduction band minima Δ_p is given by [11].

$$\Delta_p = \Delta_1(6p-3-(-1)P)/4 \quad (2)$$

An important step in this model formation is to get the control potential V_{CNT} with gate bias voltage. The knowledge of V_{CNT} is required to get the specific voltage ξ . This allows us to determine the required output parameter drain current I_D and the total charge in front of the channel of the CNTFET Q_{CNT}.

In [12], the following empirical relationship is proposed:

$$V_{CNT} = V_{GS} \quad \text{for } V_{GS} < \Delta_1 \quad (3)$$

$$= V_{GS} - £(V_{GS} - \Delta_1) \quad \text{for } VGS \geq \Delta_1$$

Where Δ_1 is the energy level for the first sub-band, and the parameter £ is given by

$$£ = £_0 + £_1 V_{DS} + £_2 V_{DS}^2 \quad (4)$$

Where £ = $£_0$, $£_1$, $£_2$ are fitting parameters depending on the gate-oxide capacitance, CNT radius , and helicity.

Now the total drain current I_D is obtained as [11].

$$I_D = 4eK_BT/h \sum_{p=0}^{+\infty}[\ln(1+\exp((-\Delta_p+V_{CNT})/K_BT))-\ln(1+\exp((-\Delta_p-\Delta p_{+}V_{CNT})/K_BT)] \quad (5)$$

Where Δp is the minima of the pth energy sub-band, e is the electron charge, K_B the Boltzman constant, h the Planck constant and T the temperature.

The gate bias V_{GS} required to produce the assumed V_{CNT} based on the electrostatic capacitance given by

$$V_{CNT} = V_{GS} - Q_{CNT}/C_{OX} \quad (6)$$

Where Cox is the gate-oxide capacitance, and Q_{CNT} depends on the number of carriers in the channel, n_{CNT}, which is the sum of the energy sub-band contributions.

It can be noted that the number of carriers n increases almost linearly as ξ becomes more and more positive and it falls off exponentially as ξ becomes negative. Hence

$$N = N_0.A.\exp \xi \quad \text{for } \xi<0 \quad (7)$$

$$= N_0 (B. \Xi + A) \quad \text{for } \xi \geq 0$$

Where the parameters A and B can be expressed empirically as polynomial of Δ [ref].

$$A = -5.3\Delta^2 + 10\Delta + 1 \quad (8)$$

$$B = 0.34\Delta + 1$$

Thus the total charge can get at the front of the channel but this charge is for a single conduction band only. The complete charge relation can be obtained by all the conduction bands that is populated by drain and source Fermi levels.

In this manner, a simplified SPICE-compatible model of CNTFET is obtained and p-type and n-type CNTFET can be obtained by only altering the polarity of the polarity [9]. Series resistance (R_S and R_D) represent metal resistances. In the next section, the SPICE compatible CNTFET model is used for all CNTFET based circuit realization.

4. Ambipolar CNTFET Behavioural Model

In addition to the MOSFET-like CNTFET model, the behavioural compact model is given in Figure.5 that allows the description of the ambipolar characteristics of SB-CNTFETs. This model is built using previously presented CNTFET model. As shown in Figure.5, an additional part has been added to the unipolar (i.e. MOSFET like) CNTFET model. The V_{DS}-I_D characteristics and V_{GS}-I_D characteristics of ambipolar CNTFET shown in Figures.6 and 7.

Figure.7 shows the ambipolar conduction for the SB-CNTFET. As outlined in [9], the symmetric bias condition at which electron and hole currents are equal, and thus total current is minimum, for mid gap SB's is always at $V_{GS} = V_{DS}/2$.

The behaviour model describes the ambipolarity and can be used to develop new architectures including both digital and analog designs [9]. The input parameters are the same as for the model of the MOSFET-Like CNTFET.

5. Results and Discussions

CNT circuit logic operation is simulated in HSPICE based on the compact model described in the section . Figure.8, 9 and 10 shows the schematic of NOT, NAND2 and NOR2 gates implementation using CNTFETs respectively. It is shown that CNTFETs are able to provide correct logical operation as MOSFET from the output waveform. It is assumed that both n-type and p-type CNTFETs have symmetrical I-V characteristics. The performance evaluation of these Boolean operations is listed in Table.1. The Figure of merit for logic devices, namely power-delay product (PDP) and energy delay product (EDP) metrics, are given

$PDP = P_{av} \times t_p;$

$EDP = PDP \times t_p$

Where P_{av} is the average power and t_p is the propagation delay. Figures and shows the PDP and EDP of CNTFET logic gates for the 45 nm process. From Table.3, it is found that NAND3 and NOR3 has the largest propagation delay since both of them has multiple fan-in and fan-out each.

6. Conclusions

In this research work, the SPICE compatible circuit modified model for CNTFET using HSPICE has been developed. Using this developed model, the performance of the basic logic gates like NOT, NOR2, NAND2, NOR3 and NAND3 have been evaluated. These logic gates are simulated in HSPICE and characterized in terms of PDP and EDP. It has been found that NAND3 or NOR3 has the largest propagation delay since both of them has multiple fan-in and fan-out each. The design of complex analog and digital circuits based on ambipolar CNTFETs for communication applications will be described in a paper which will be communicated very shortly.

7. ACKNOWLEDGMENTS

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8. REFERENCES

[1] McEuen. E., Fuhrer.M.S., and Park.H., Single –Walled Carbon Nanotube Electronics, 1(2002), 78-85.

[2] Yang. L., Anantram.P., Han.J. and Lu.J.P., Band-gap Change of Carbon Nanotubes: Effect of small Uniaxial and Torosional Strain, Phys. Rev.B, 60, 19(1999), 13874-13878.

[3] Guo.J, Datta.S. and Lundstorm.M, Assessment of Silicon MOS and Carbon Nanoyube FET Perofrmance limits using a general theory of ballistic transistors, Digest IEDM (2000)711-715.

[4] Wind.S, Appenzeller.J. and Avouris. Ph., Vertical Scxaling of Carbon Nanotube Field Effect Transistors using Top Gate Electrodes, Appl. Phys. Letter, 80 (2002)3817-3819.

[5] Javey.A. et. Al, Ballistic Carbon Nanotube Field Effect Transistor, Nature, 424(2003), 654-657.

[6] Lin.Y.M., Appenzeller.J and Avouris.Ph, Novel Carbon Nanotube FET design with tunable polarity, Electron Devices Meeting, IEDM Technical Digest, IEEE Int. (2004), 687-690.

[7] Guo.J., Javey.A and Lundstrom.M, Performance Analysis and Design Optimism of near sballistic carbon Nanotube FETs, IEDM Tech. Digest (2004), 703-706.

[8] Yang Xuebei and Mohanram Kartik, Ambipolar Electronics, Rice University Technical Report, TREE1002(2010)

[9] O'Connor. I et.al, CNTFET Modeling and Reconfigurable Logic Design, IEEE Tran. Circuit and Systems I, 54 (2007), 2365-2379.

[10] Raychowdhury.A et.al, A Circuit-Compatible Model of Ballastic Carbon Nanotube Field Effect Transistors, IEEE Trans. Computer-Aided Design, 12, 10 (2004), 1411-1420.

[11] Guo.J., Lundstrom.M. andvDatta.S., Performance Projections for Ballistic Carbon Nanotube Field Effect Transistors, Appl. Phys. Letters, 80, 17 (2002) 3192-3194.

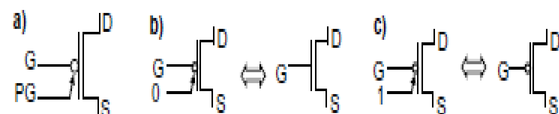

Figure 1: Ambipolar CNTFET: device symbol (a), configuration as n-type (b) and p-type (c).

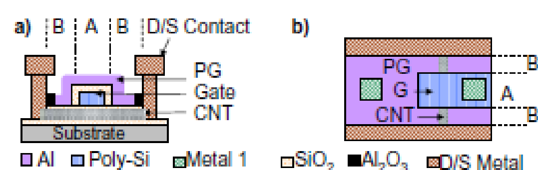

Figure 2: Ambipolar CNTFET device: a) Layout b) Symbol

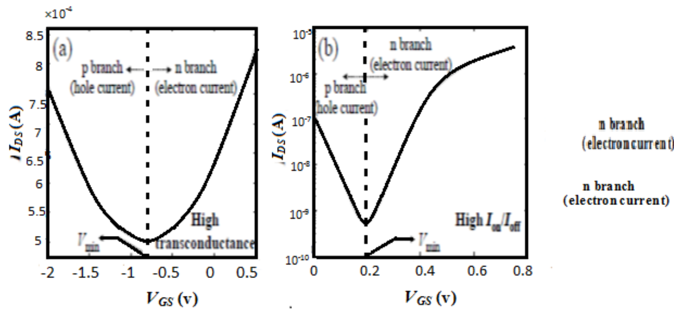

Fig 3: I-V characteristic curves of Ambipolar CNTFET

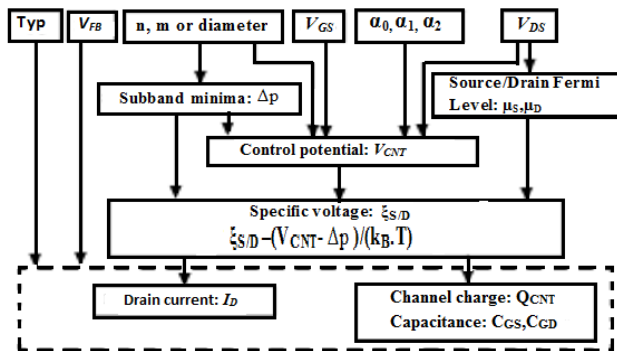

Figure.4 : Computational procedure to evaluate the drain current $I_{D\ for}$ CNTFET Model.

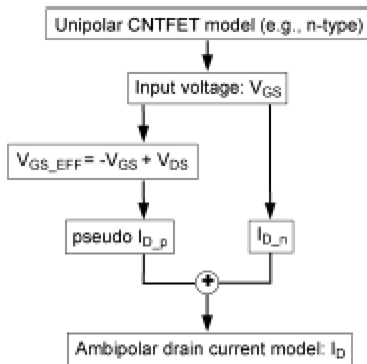

Figure.5: Ambipolar CNTFET Behavioural Model

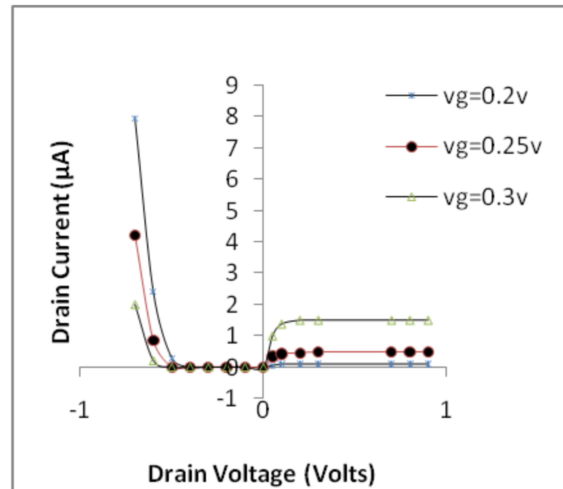

Fig 6: I-V characteristic curves of Ambipolar CNTFET for different gate voltages with fixed dielectric constant, k=16.

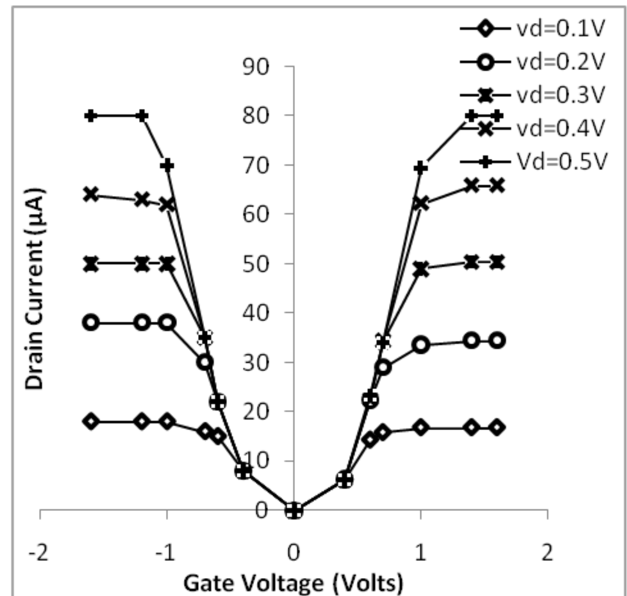

Fig 7: Transfer characteristic curves of Ambipolar CNTFET for different drain voltages with fixed dielectric constant, k=16

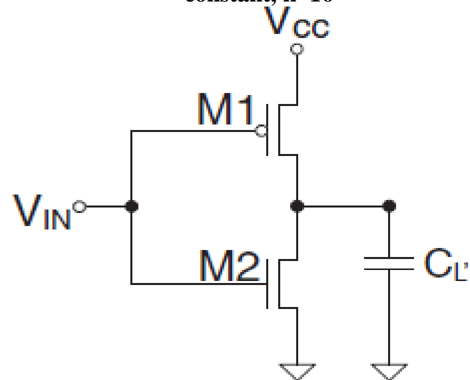

Figure.8: NOT gate using CNTFET.

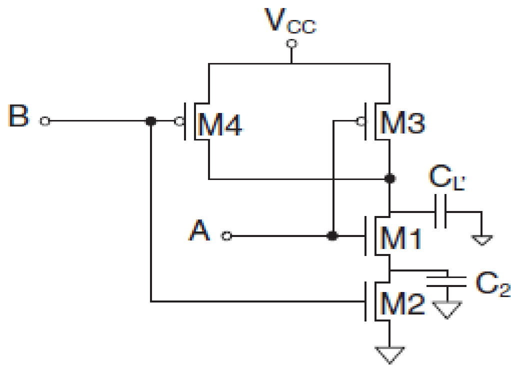

Figure.9 : Two Input NAND Gate using CNTFET

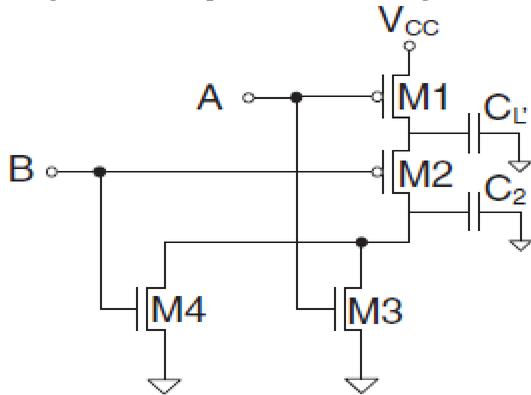

Figure.10: Two Input NOR gate using CNTFET

TABLE.1
AVERAGE DELAY, POWER, POWER –DELAY-PRODUCT (PDP) AND ENERGY-DELAY-PRODUCT (EDP) FOR CNTFET BASED DESIGNS.

Logic block	Power (J/s)	Delay (ns)	PDP (J)	EDP (J-s)
Inverter	0.11e-9	15	20e-18	1e-28
NAND	2 0.6e-9	30	18e-18	1.2e-28
NOR2	0.55e-9	40	22e-18	1.4e-28
NAND3	0.33e-9	55	20e-18	1.3e-28
NOR3	0.47e-9	45	21e-18	1.2e-28